

## GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8  
DP + DP + DP + HDMI/DP

## TABLE OF CONTENTS

## Page Description

1	Table of Contents
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	MEMORY: GPU PARTITION A/B
5	MEMORY: FBA PARTITION[31:0]
6	MEMORY: FBA PARTITION[63:32]
7	MEMORY: FBB PARTITION[31:0]
8	MEMORY: FBB PARTITION[63:31]
9	MEMORY: GPU PARTITION C/D
10	MEMORY: FBC PARTITION[31:0]
11	MEMORY: FBC PARTITION[63:32]
12	MEMORY: FBD PARTITION[31:0]
13	MEMORY: FBD PARTITION[63:32]
14	MEMORY: GPU PARTITION E/F
15	MEMORY: FBE PARTITION[31:0]
16	MEMORY: FBE PARTITION[63:32]
17	MEMORY: FBF PARTITION[31:0]
18	MEMORY: FBF PARTITION[63:32]
19	GPU GND, RFUs & RSVD
20	GPU POWERS
21	GPU: NVVDD DECOUPLING
22	GPU: FBVDD DECOUPLING
23	GPU: MSVDD DECOUPLING
24	BLANK
25	NVHS x16

## Page Description

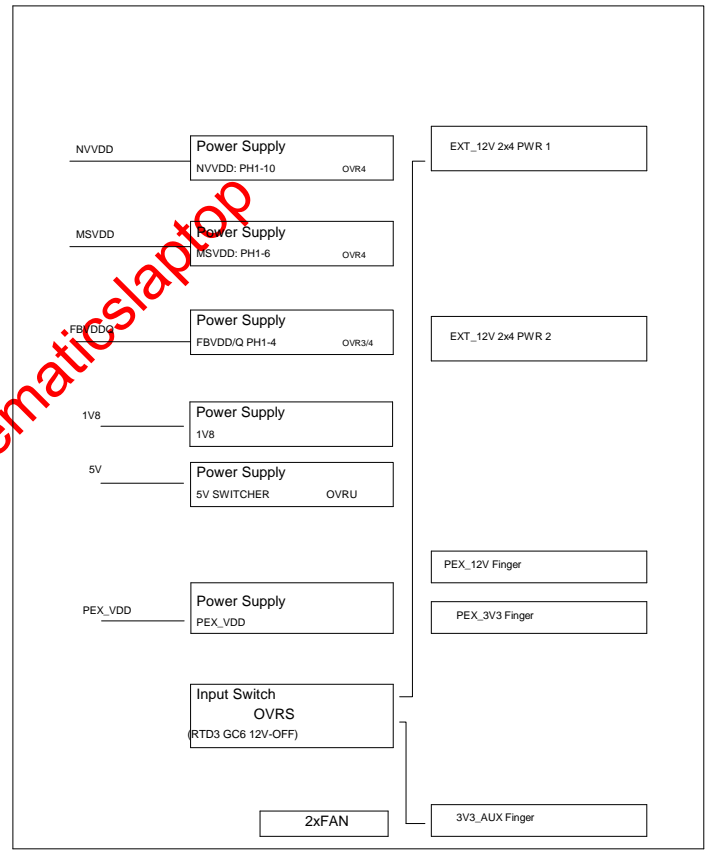
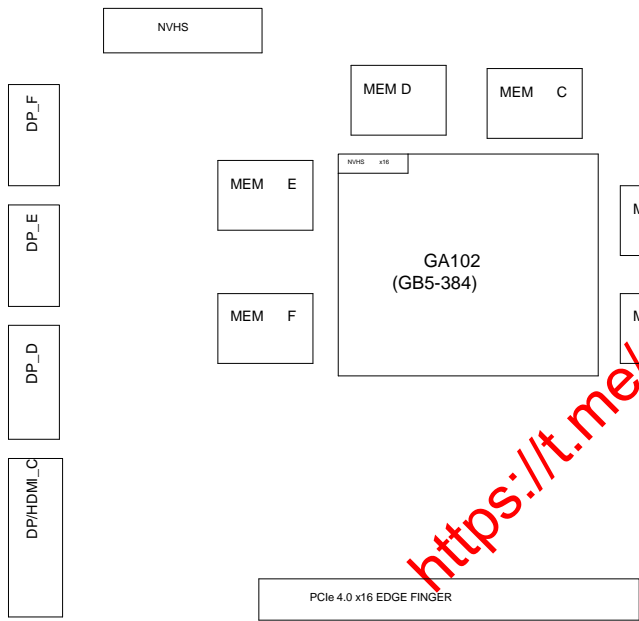
26	MISC: THERMAL, JTAG, GPIO
27	IFPA UNUSED, IFPB UNUSED
28	IFPE DP
29	IFPD DP
30	IFPC HDMI/DP
31	IFFF DP
32	MISC. ROM, STRAPS
33	MISC. XTAL, PLL
34	PS: 5V
35	PS: PEX_DVDD and 1V8
36	BLANK
37	PS: FBVDD Controller OVR3
38	PS: FBVDDQ OVR4
39	PS: FBVDD PH1
40	PS: FBVDD PH3
41	PS: FBVDD PH2
42	PS: FBVDD PH4
43	PS: FBVDD OUTPUT CAP
44	PS: MSVDD CONTROLLER
45	PS: MSVDD PH1
46	PS: MSVDD PH2
47	PS: MSVDD PH3 and PH5
48	PS: MSVDD PH4 and PH6
49	PS: MSVDD OUTPUT CAP(TOP)
50	BLANK

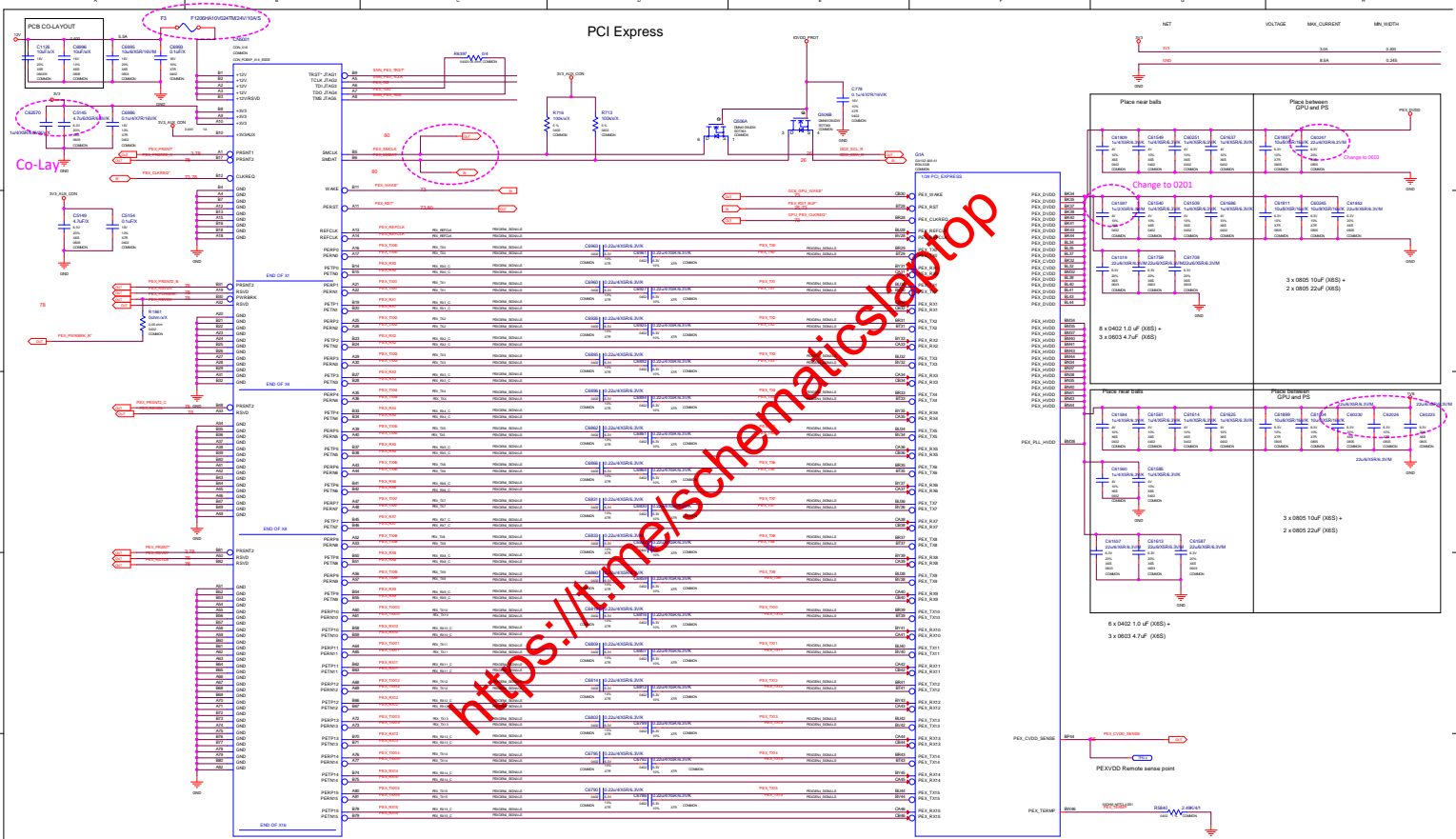
## Page Description

51	PS: NVVDD Controller_OVR8
52	PS: NVVDD PH1 (PWM1)
53	PS: NVVDD PH2 (PWM6)
54	PS: NVVDD PH3 (PWM3) and PH4 (PWM3)
55	PS: NVVDD PH5 (PWM7) and PH7 (PWM8)
56	PS: NVVDD PH6 (PWM7)
57	PS: NVVDD PH8(PWM5) and PH9(PWM2)
58	PS: NVVDD PH10 (PWM4)
59	Colayout Notes
60	BLANK
61	PS: NVVDD OUTPUT CAP(TOP)
62	BLANK
63	PS: INPUT SWITCH RTD3
64	BLANK
65	PS: INPUTS, FILTERING, and, MONITORING
66	PS: HOT UNPLUG
67	PS: Discrete Power Steering
68	PS: PREFILTER
69	PS: PREFILTER B
70	Sequence: 5V, 1V8, 3V3_SEQ
71	Sequence: NV, PEX, FB EN
72	Sequence: 3V3 MONITOR
73	Sequence: MISC
74	MISC: LED & FAN
75	RGBW LED REF

<https://www.gigabyte.com/laptops>

# Block Diagram

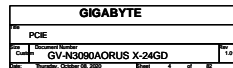


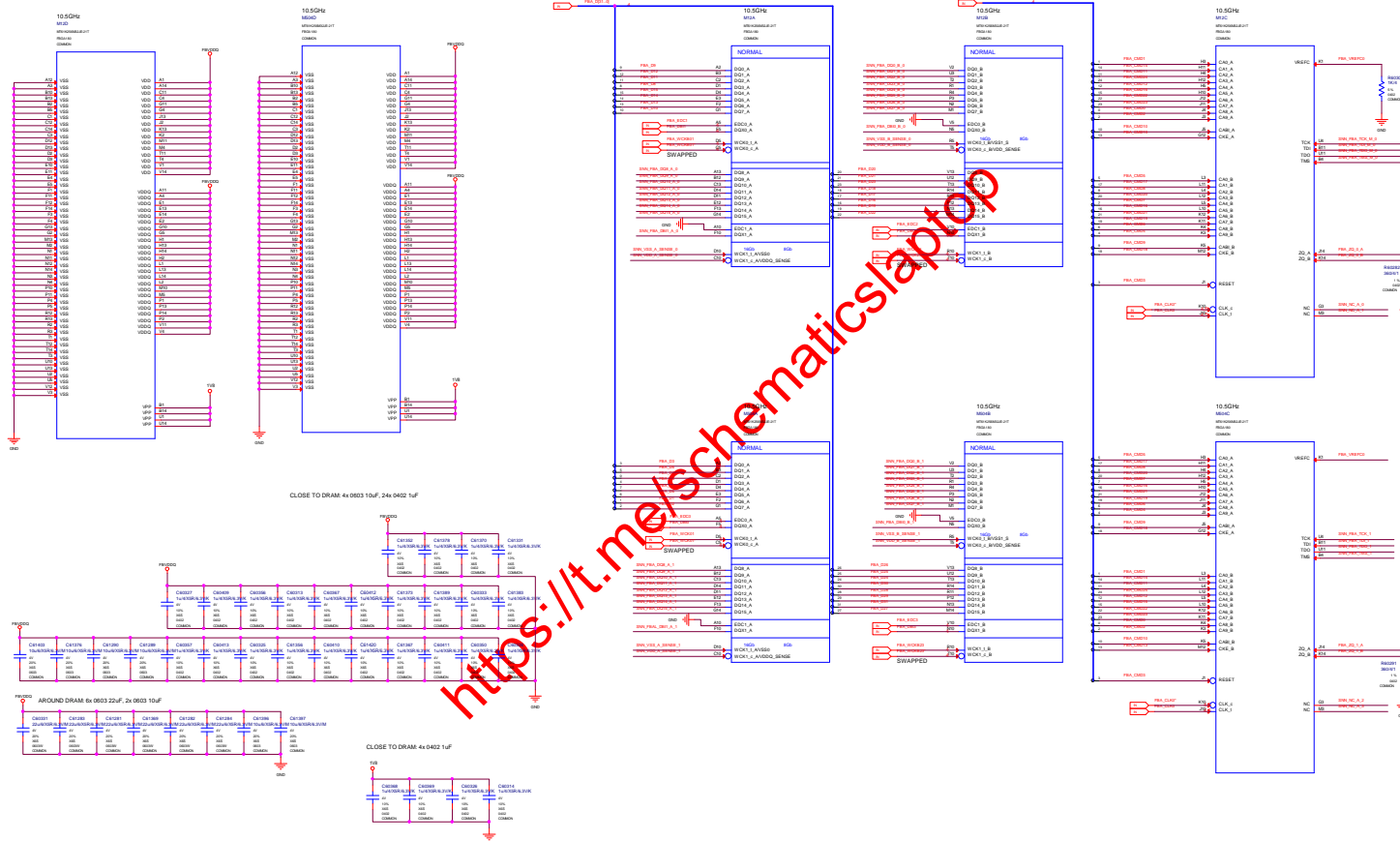


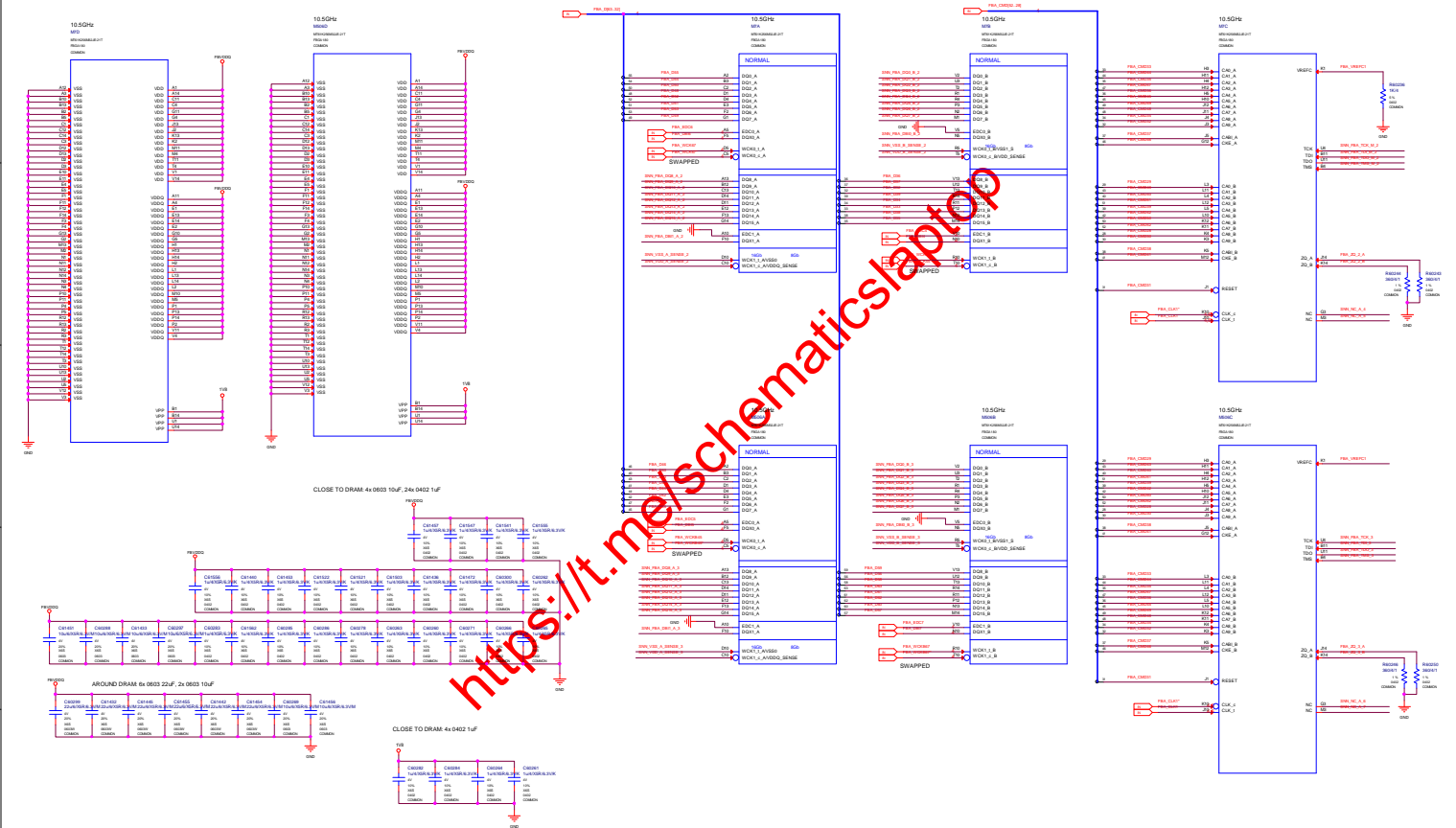
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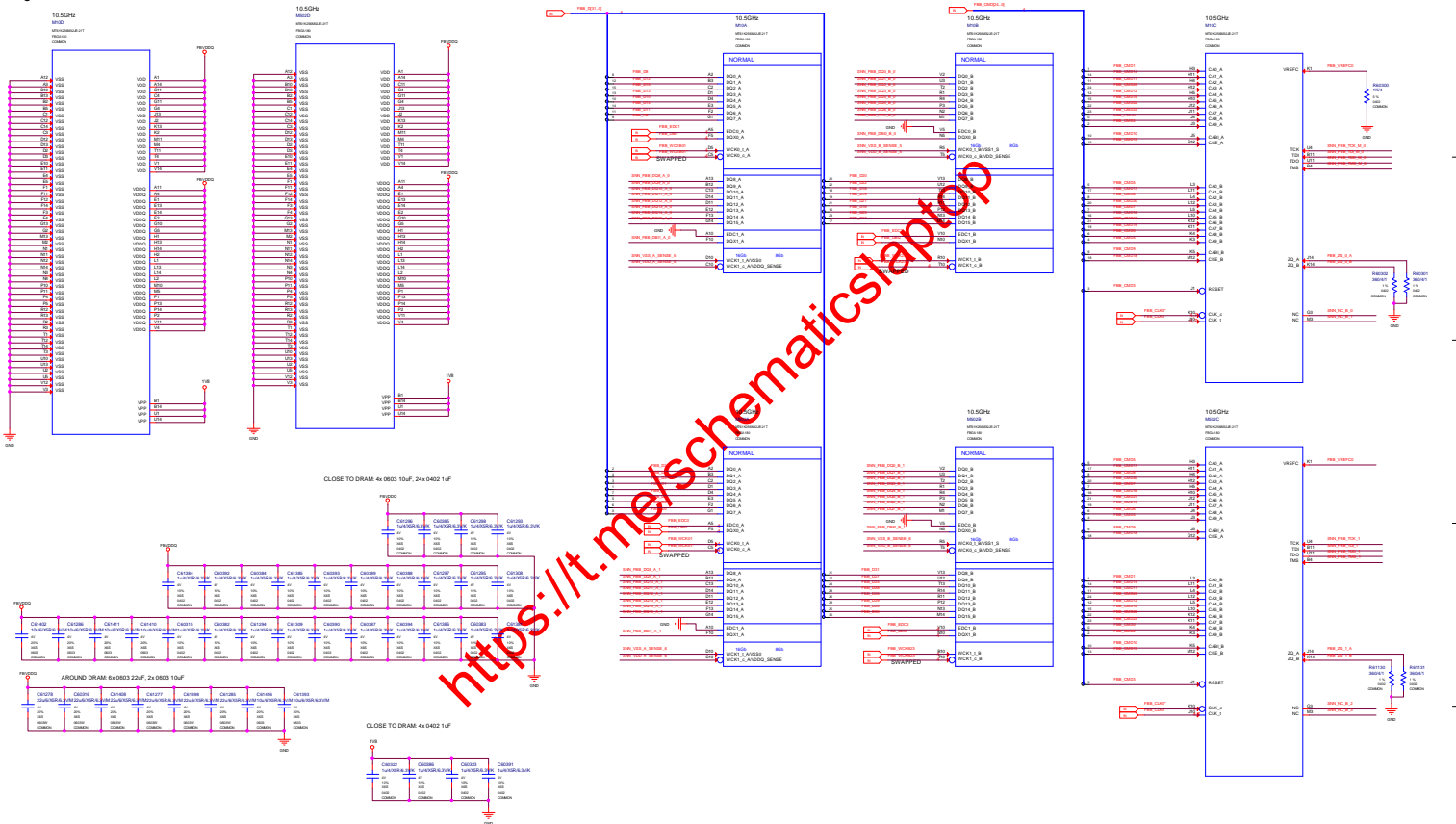
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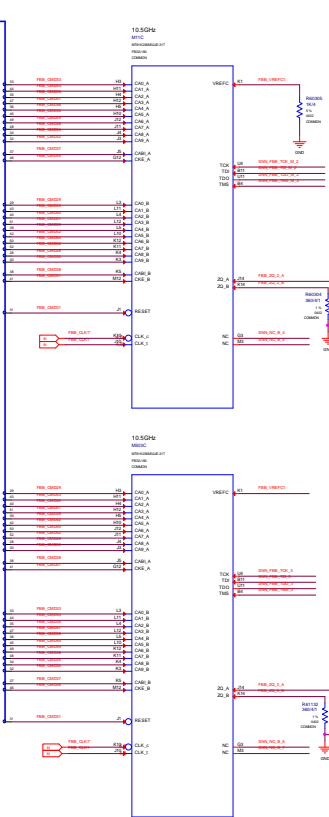
GIGABYTE	
PCB	
Model	GV-N3080AORUS X-24GD
Version	1.00



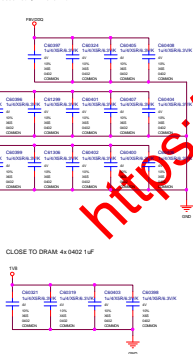




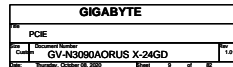


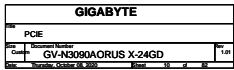


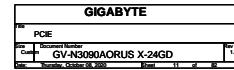
CLOSE TO DRAM 4x 0402 1uF

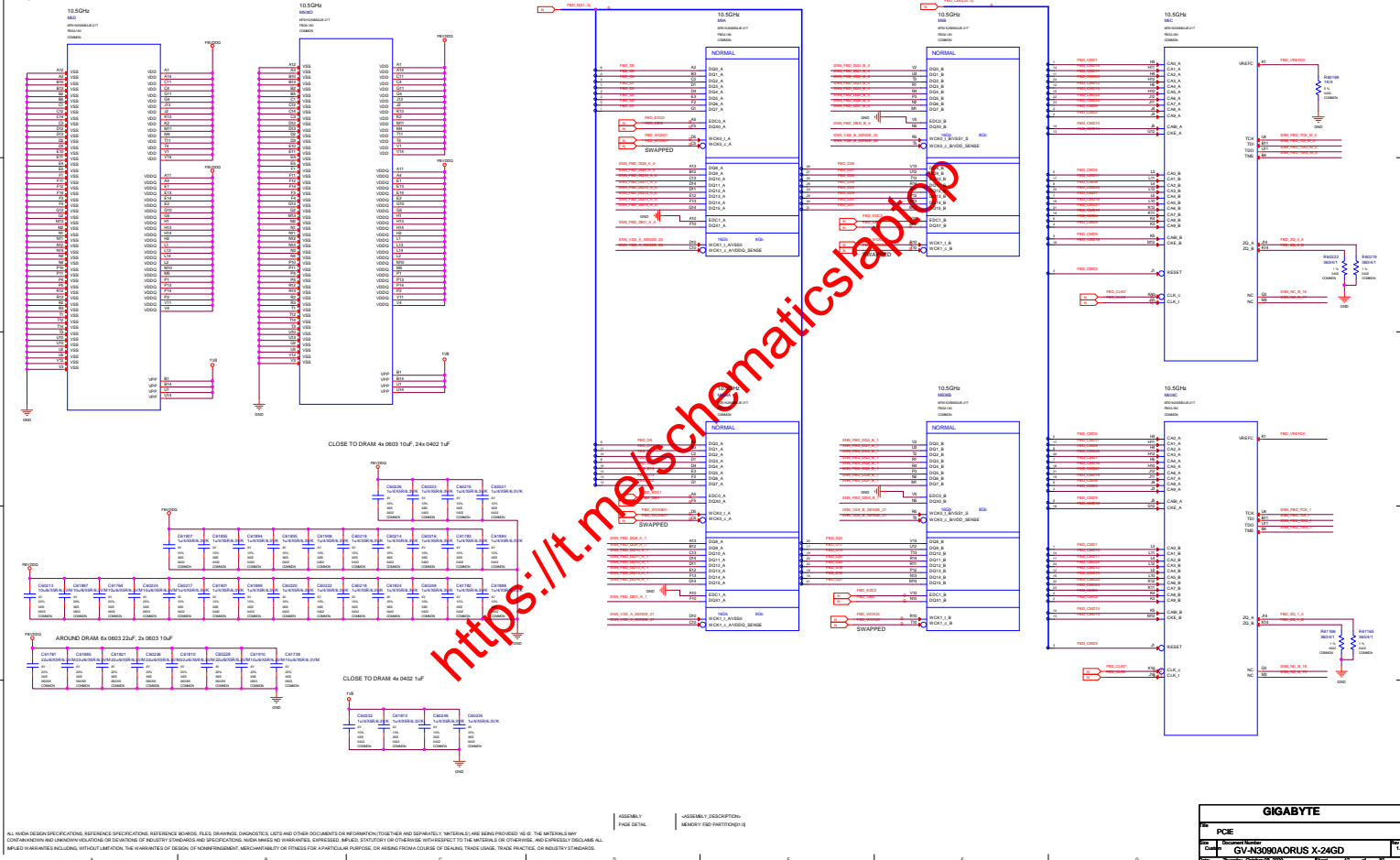


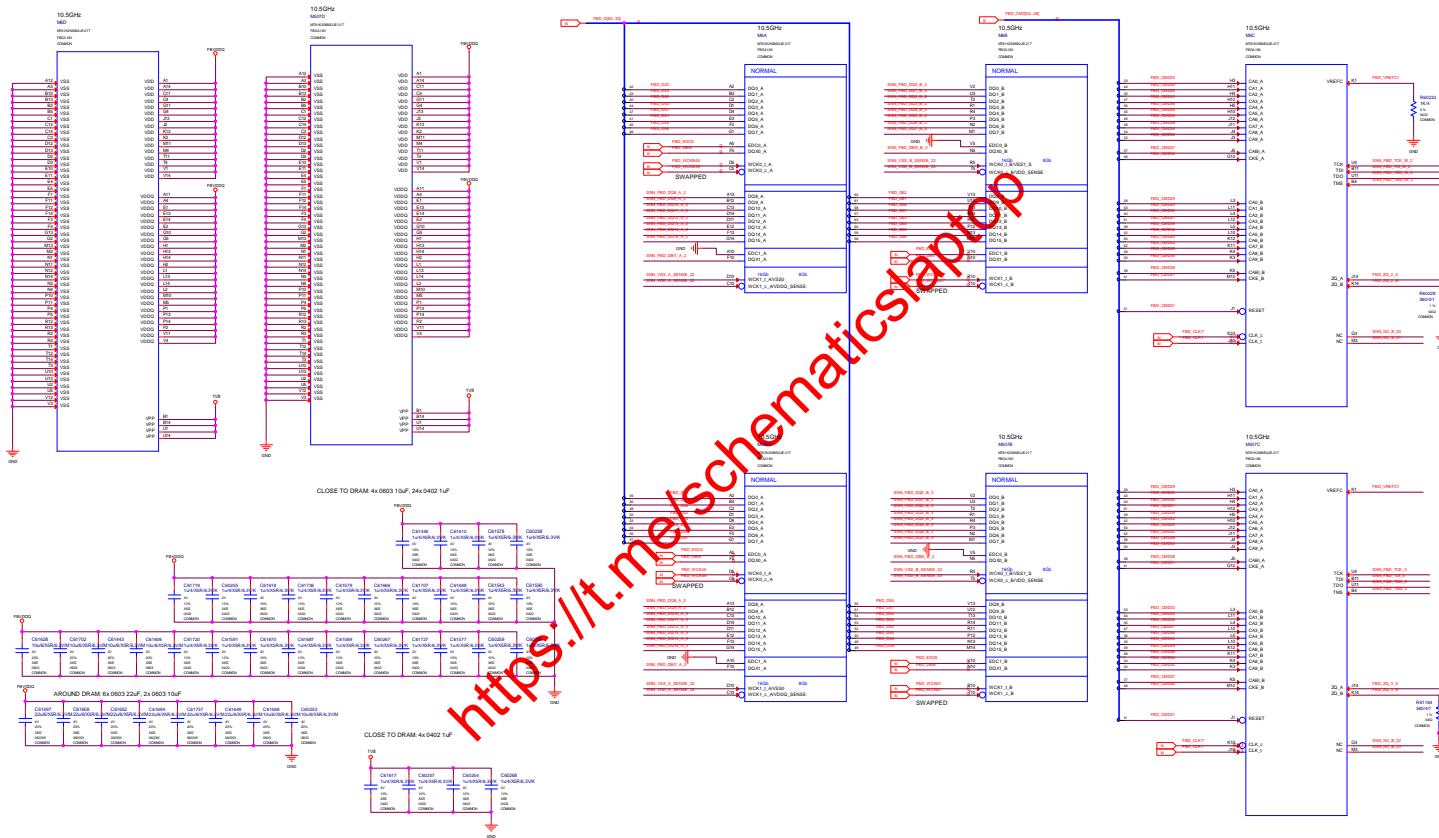




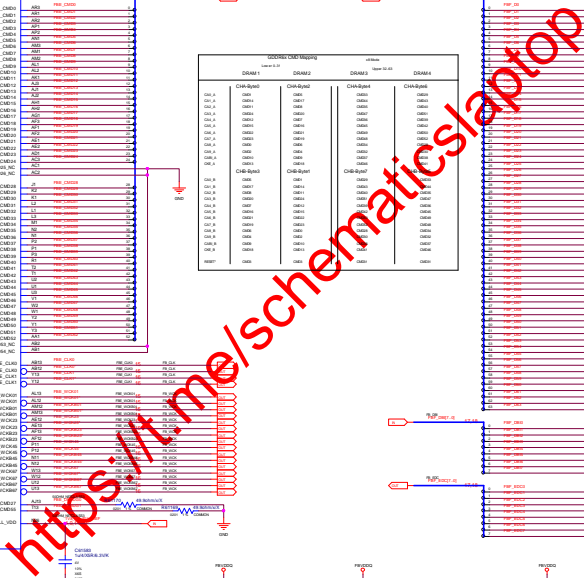




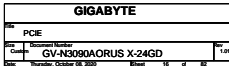




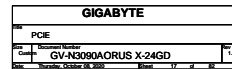
RESET

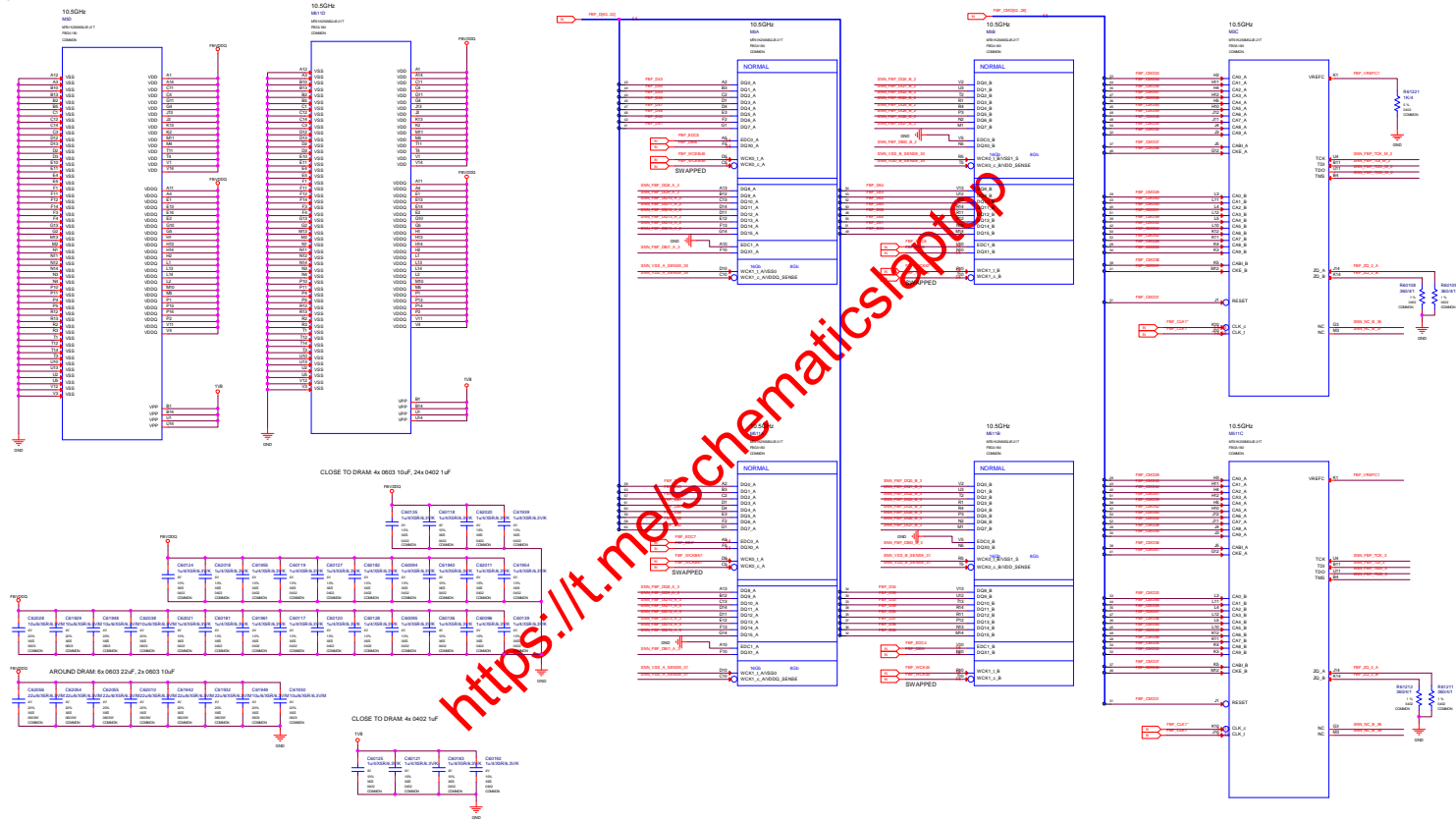












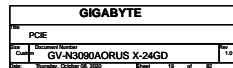
## GPU GND, RFUs &amp; RSVD



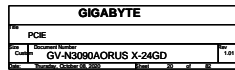
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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION:  
GPU GND, RFUs & RSVD



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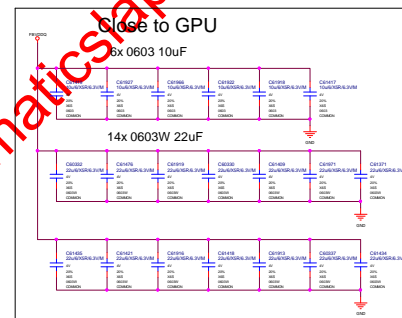
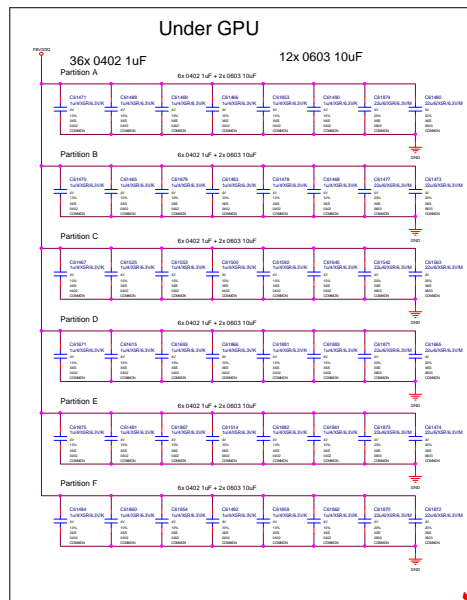


## NVVDD

## UNDER GPU



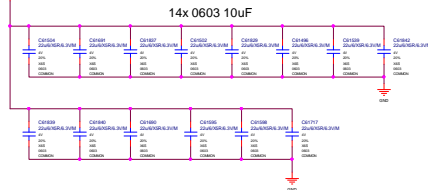
## FBVDDQ



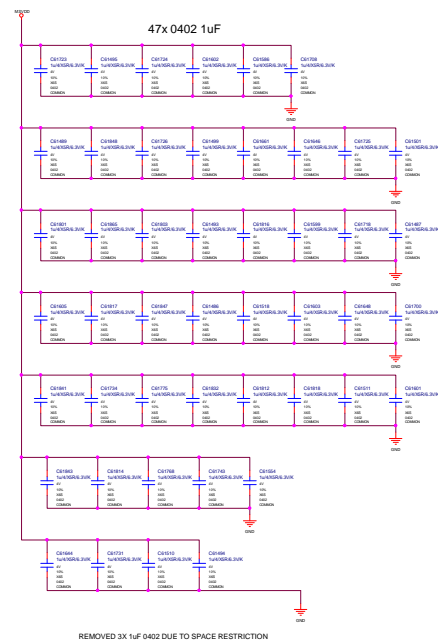
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## MSVDD

## UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



<https://t.me/schematics4laptop>

GIGABYTE

PCIE		Description	
Cap	GV-N3090AORUS X-24GD	Model	1.01
Rev. 1.0.0.0 (2024-08-08)		Rev. 1.0.0.0 (2024-08-08)	Rev. 1.0.0.0 (2024-08-08)

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GIGABYTE	
PCIE	
GV-N3090AORUS X-24GD	
Rev 1.01	



# NVHS Interface and FRAME LOCK



BRIDGE POR

LED -> NO

ID ROM -> YES



REMOVE ONE BECAUSE OF NO LIMITATION



REMOVE ONE BECAUSE OF NO LIMITATION



REMOVE ONE BECAUSE OF NO LIMITATION



REMOVE ONE BECAUSE OF NO LIMITATION



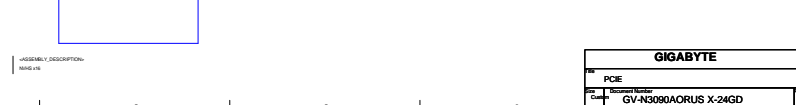
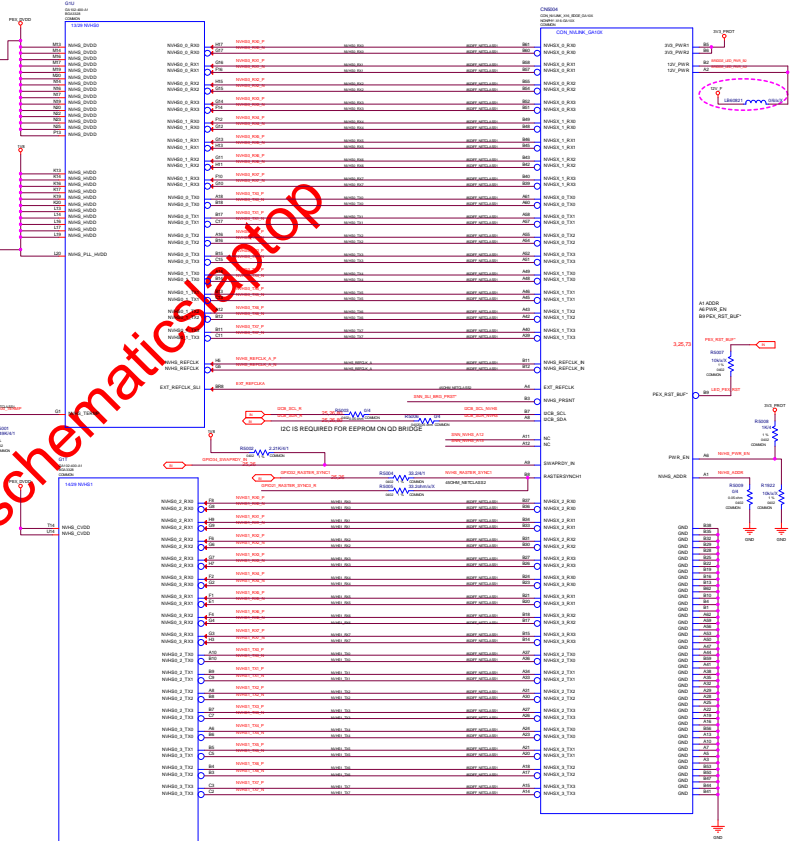
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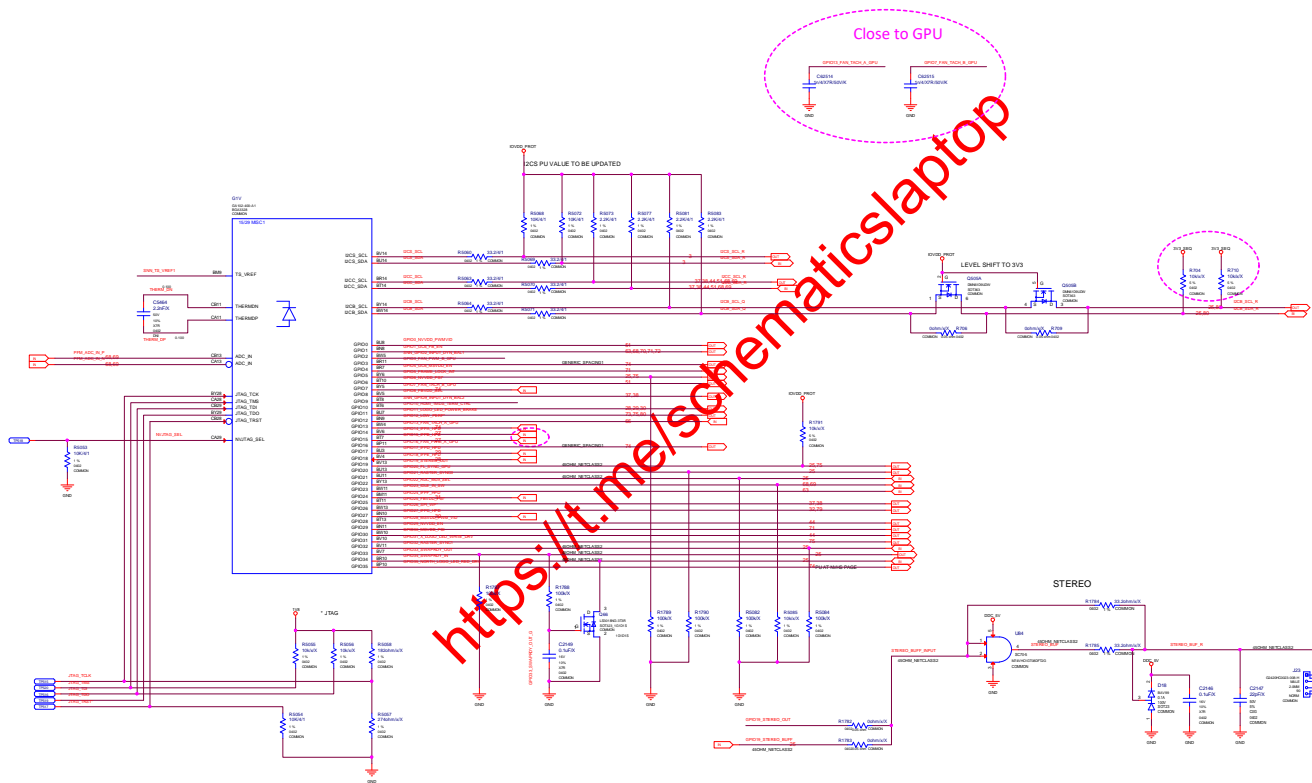
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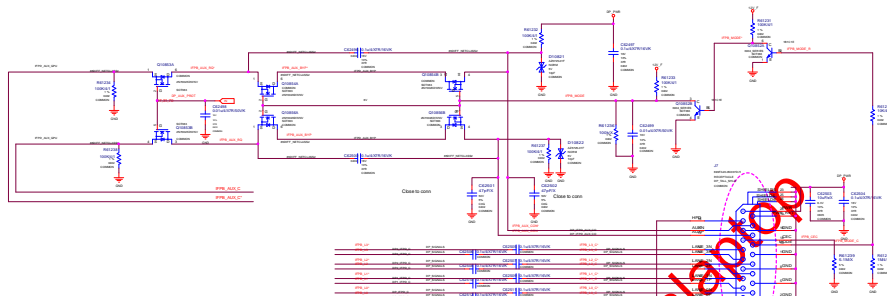


# MISC1: Fan, Thermal, JTAG, GPIO, STEREO

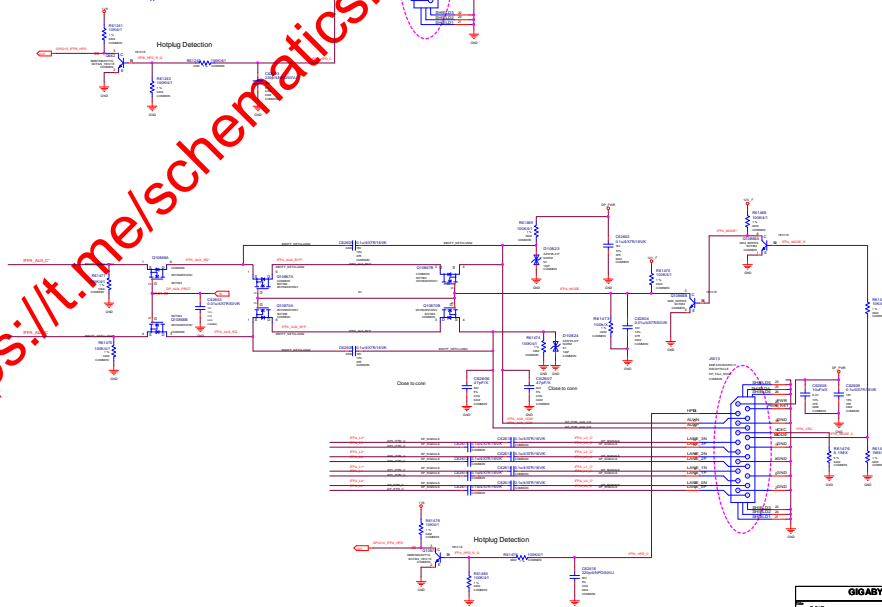
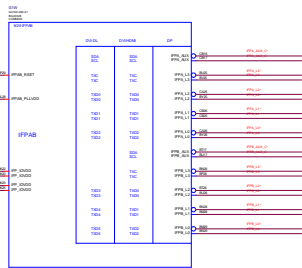
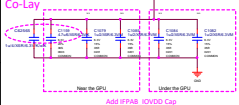


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# IFPA, IFPB For DP x2

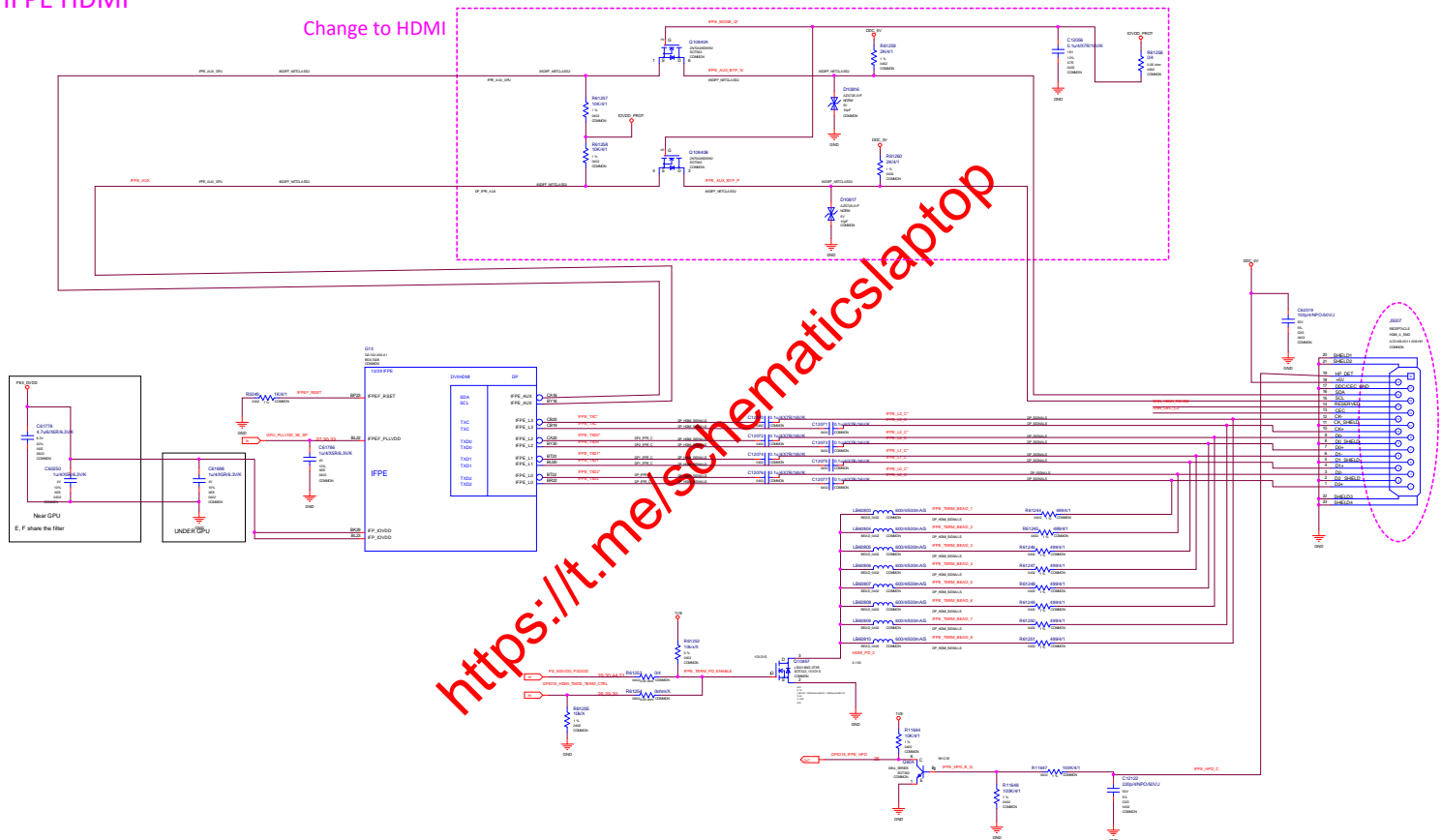


Co-Lay



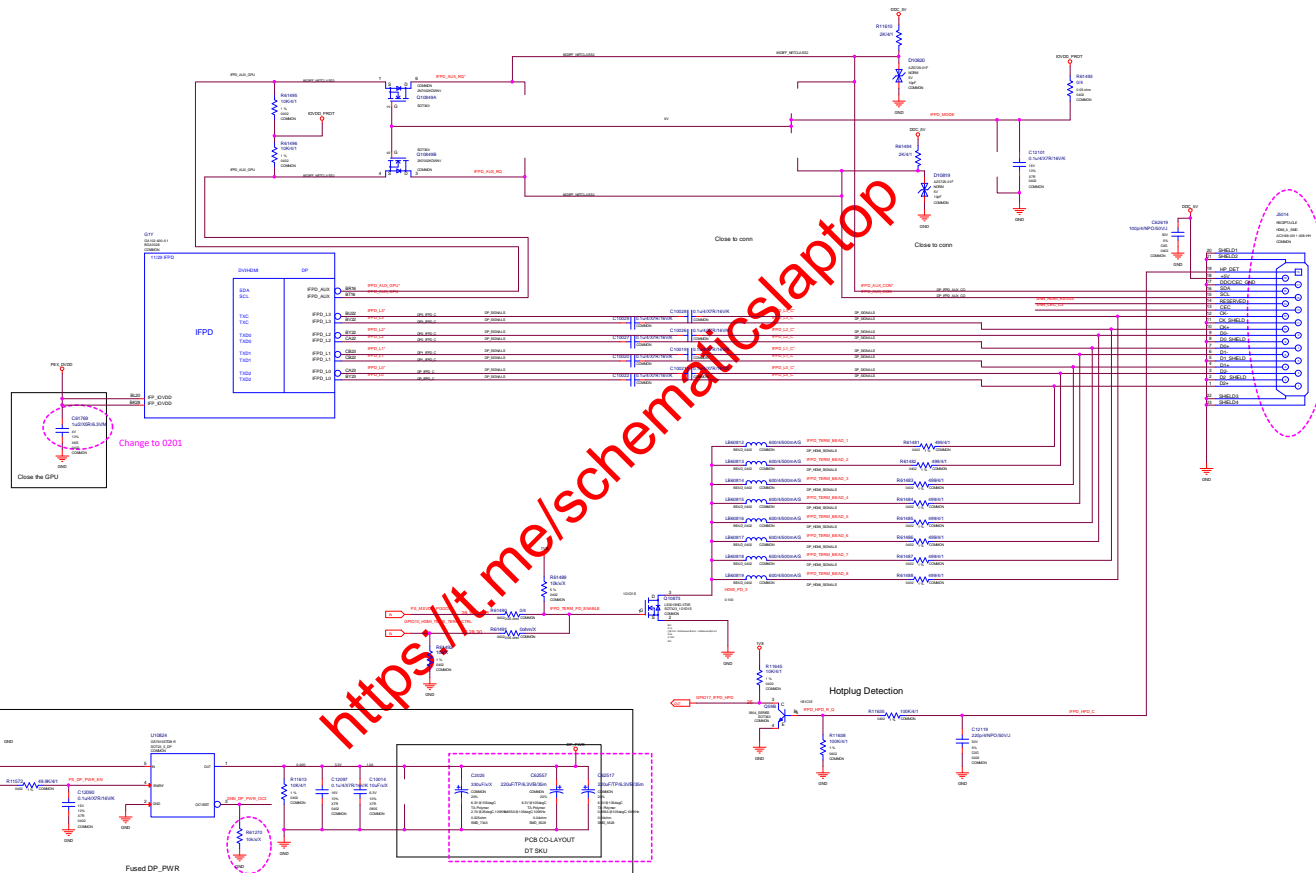
# IFPE HDMI

Change to HDMI



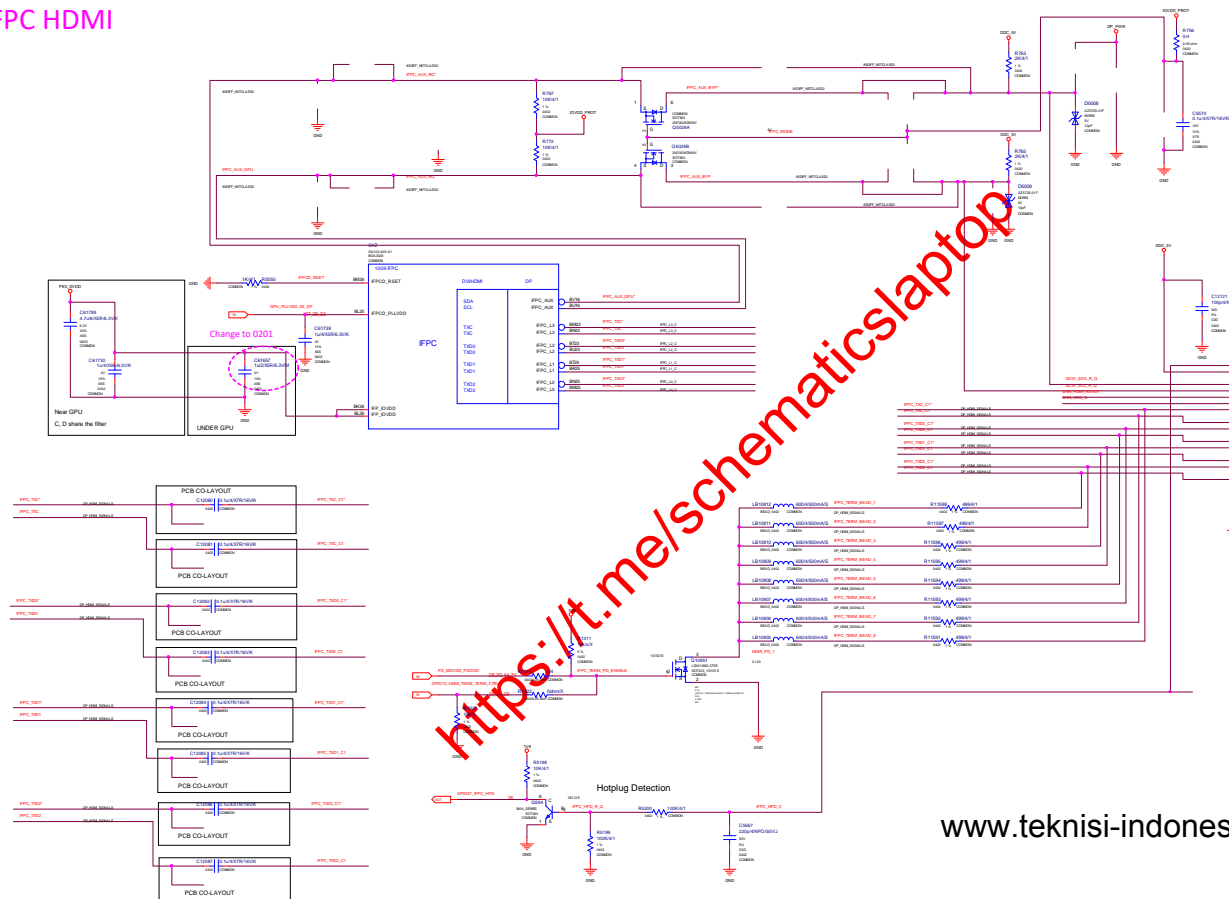
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## IFPD HDMI



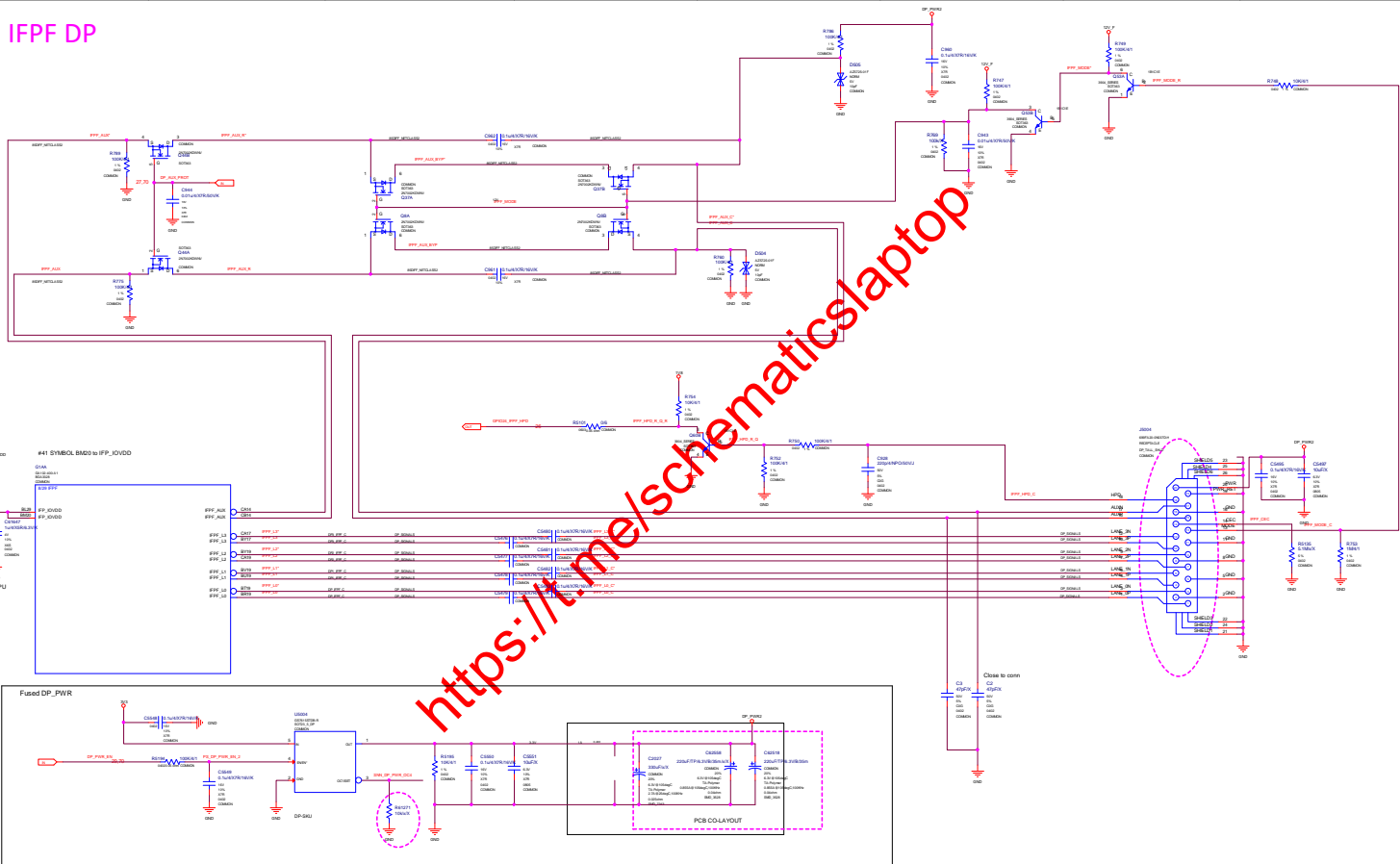
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# IPMC HDMI



www.teknisi-indonesia.com

# IFPF DP



<https://t.me/schematics4laptop>

# MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps	
L	H	L	00010	RAMCFG TBD	
H	L	L	00100	RAMCFG TBD	
H	L	H	00101	RAMCFG TBD	
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps	DEFAULT

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

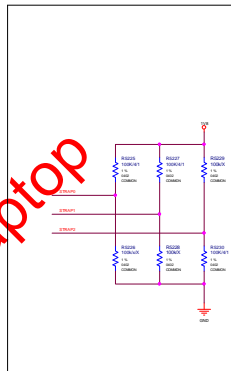
ROM_SO	ROM_SI	ROM_SCLK	SMARTFANPULSEFS_OVERT	1:ENABLE 0:DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
L	L	L	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	L	1	1	1	1
M	H	L	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	
L	H	L	0	0	1	
L	L	H	0	0	0	
L	L	L	0	0	0	

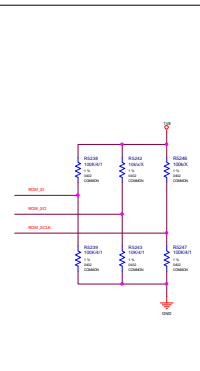
Default

- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE VGA
- 0:VGA\_DEVICE DISPLAY

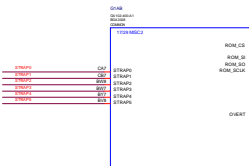
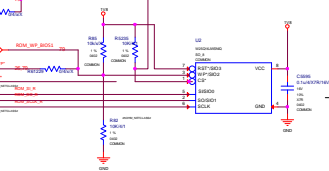
GROUP0



GROUP1



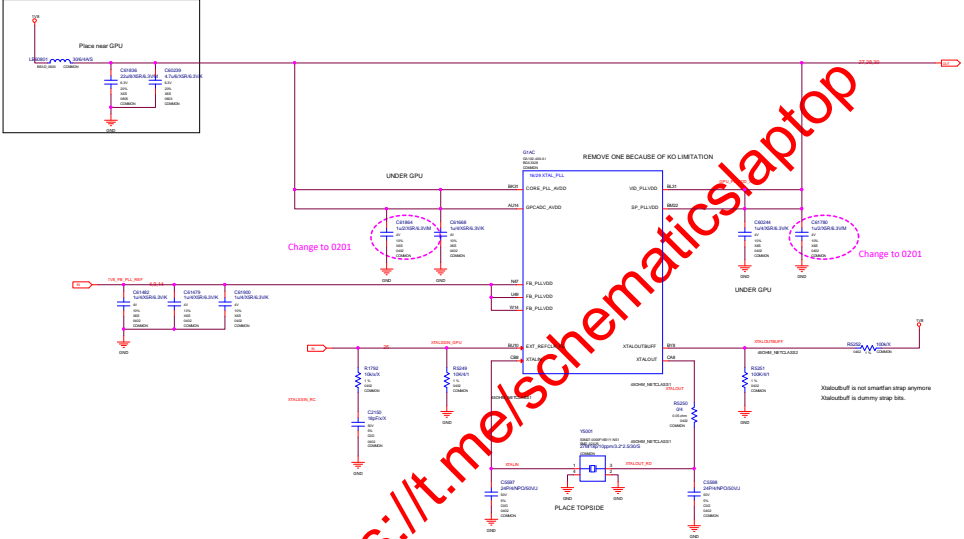
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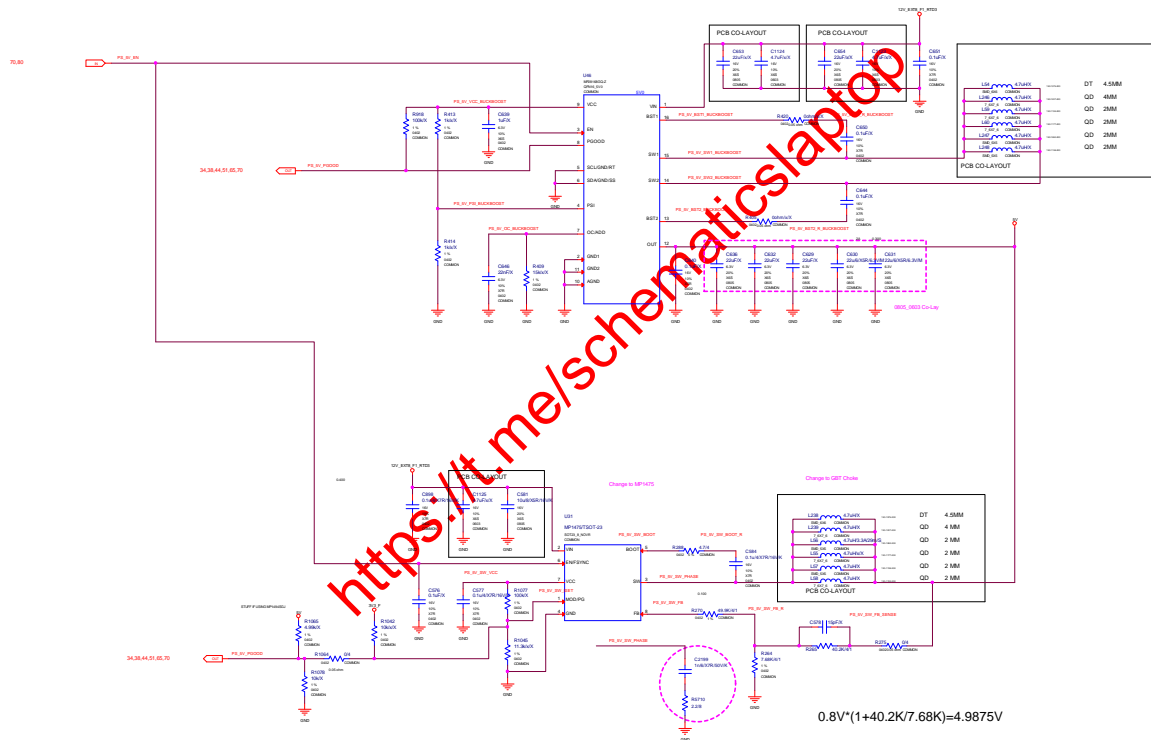


Modify



MISC: XTAL. PLL







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GIGABYTE

PCIE

GV-N3090AORUS X-24GD

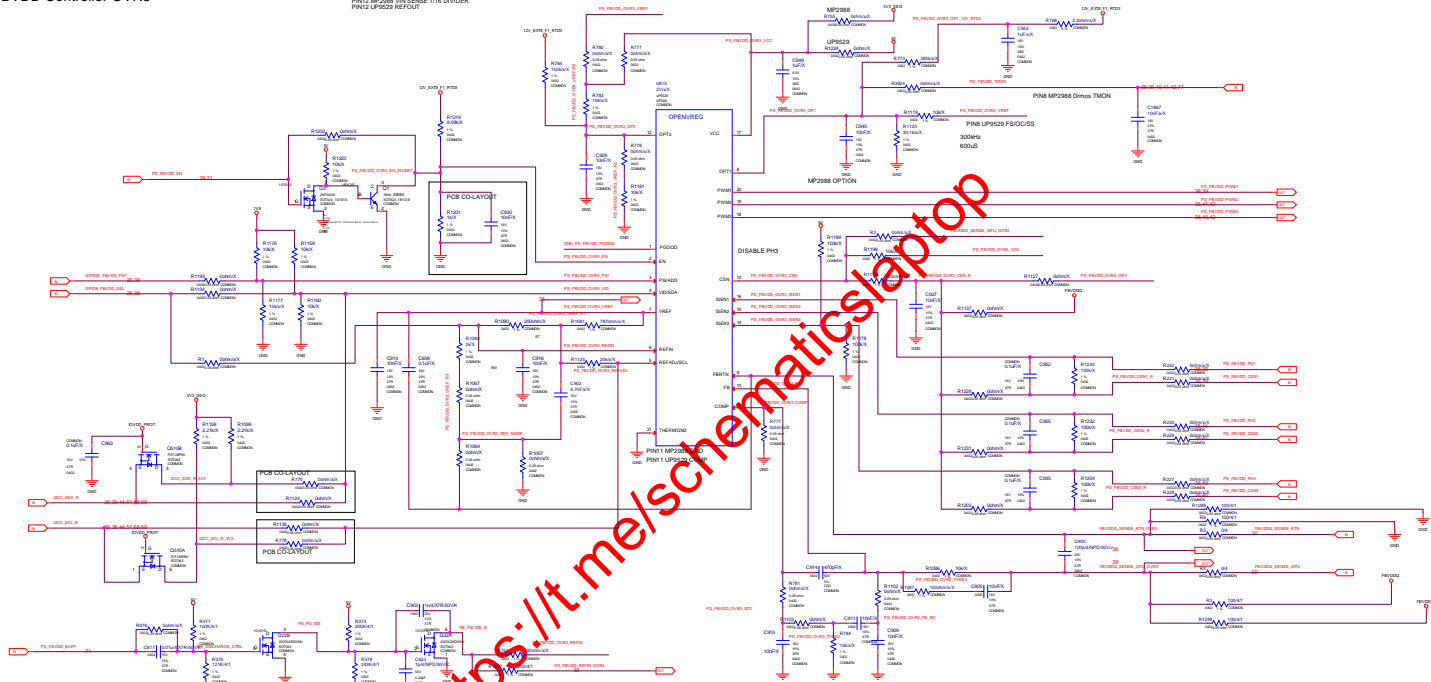
Rev. 1.01

Rev. 1.01

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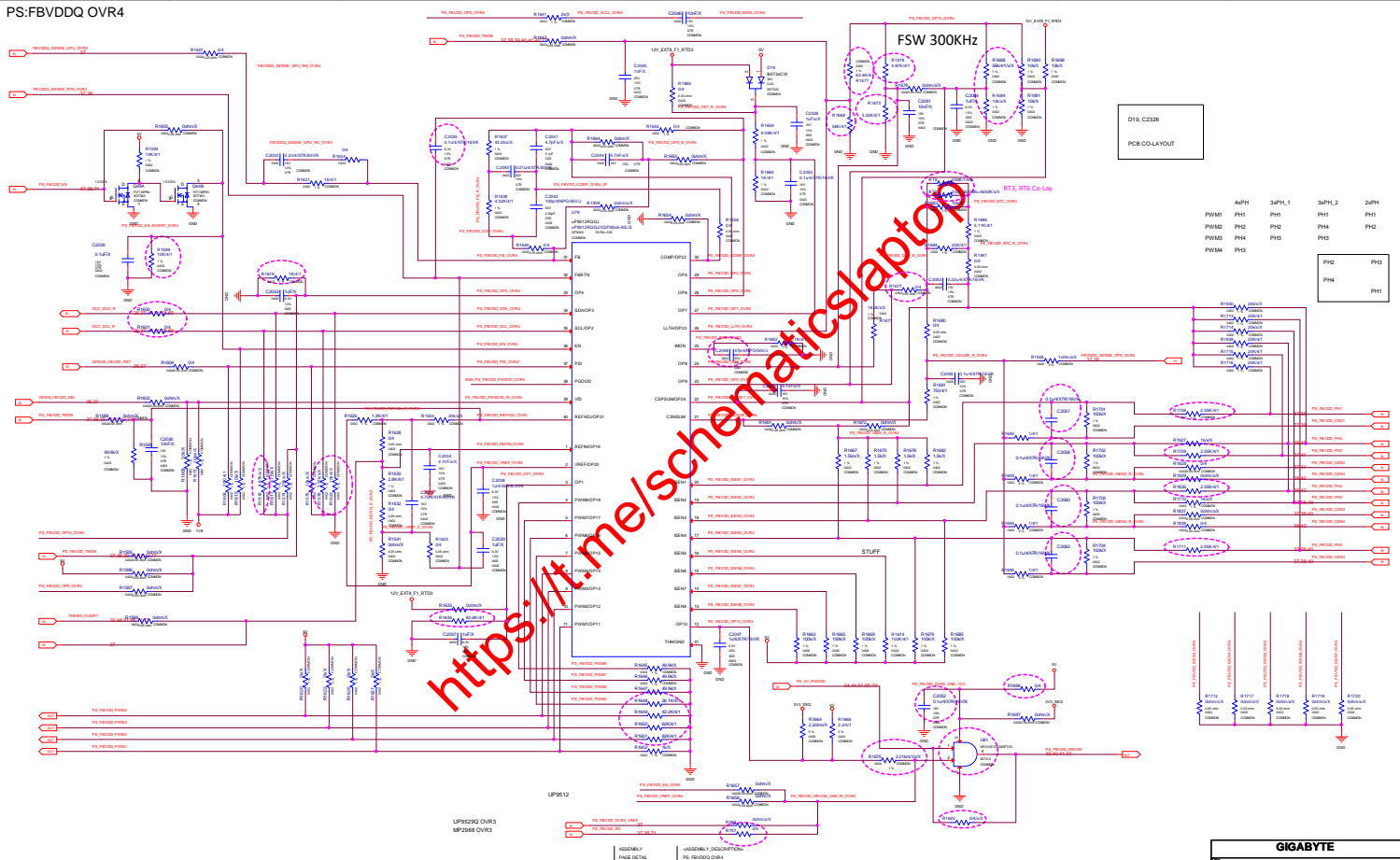
# PS: FBVDD Controller OVR3

PN12 MP2588 VIN SENSE 1/16 DIVIDER  
PN13 UP529 FS/OCS



FOR DT SKU

## PS:FBVDDQ OVR4



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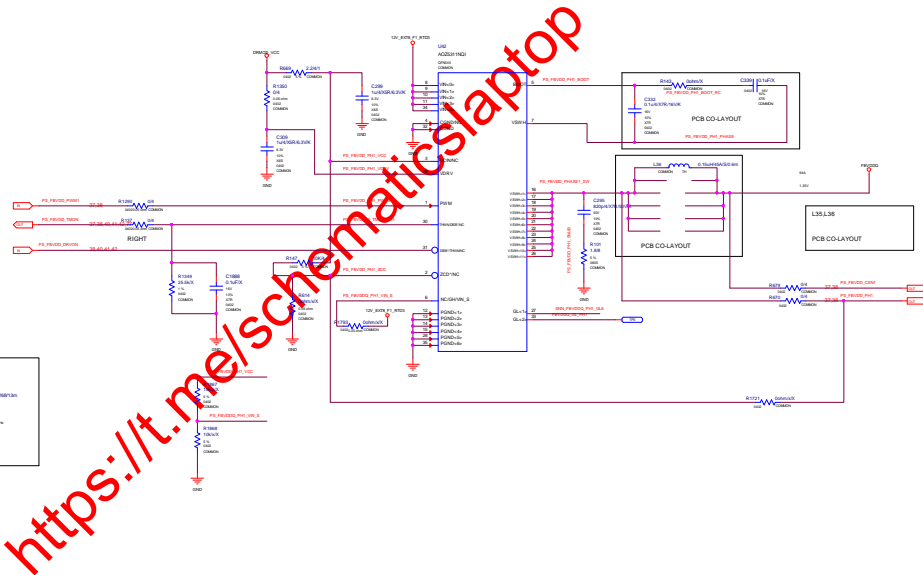
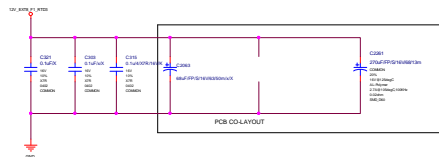
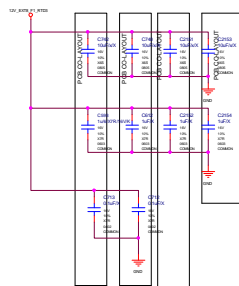
## GIGABYTE

BCI

Document Number	GV-N3090AORUS X-24GD
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7

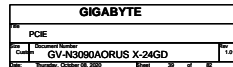
PS: FBVDD PH1



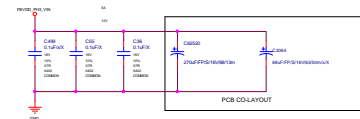
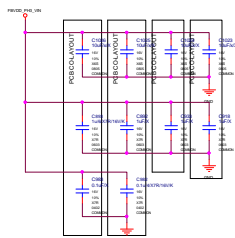
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ASSEMBLY  
PAGE DETAIL

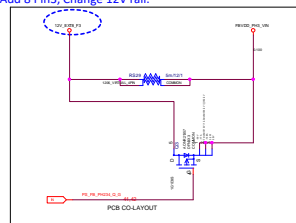
ASSEMBLY DESCRIPTION  
PS: FBVDD PH1



## PS: FBVDD PH3



Add 8 Pin3, Change 12V rail.



## FBVDD PH3 INPUT ANTI-BACKDRIVE

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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
PS: FBVCO Pkg

## GIGABYTE

PC

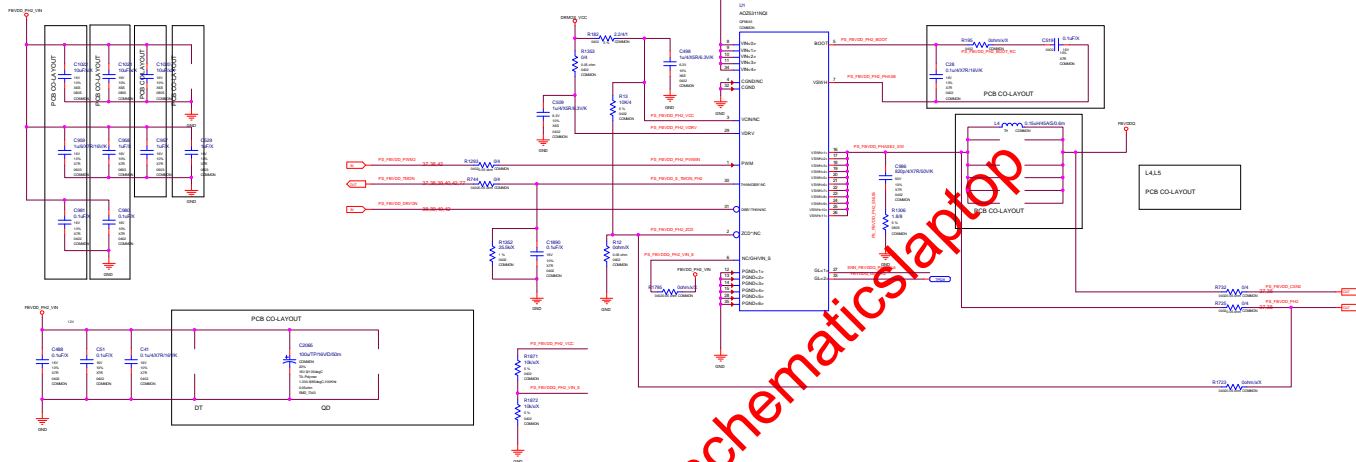
Document Number  
GV-N3090AORUS X-24GD

Author:  Title:

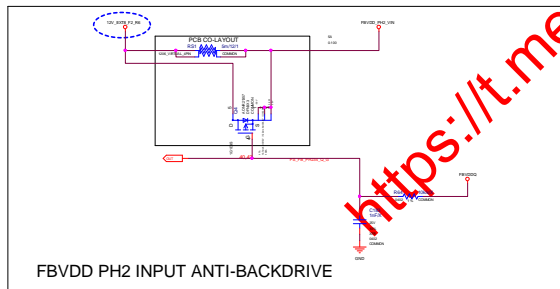


## PS: FBVDD PH2

Add 8 Pin3, Change 12V rail.



Add 8 Pin3, Change 12V rail.



### FBVDD PH2 INPUT ANTI-BACKDRIVE

The schematic diagram illustrates the internal circuitry of a Pico-2 board. Key components and connections include:

- Power Management:** A 3.3V regulator (LDO33) and a 5V regulator (LDO5V) are shown, along with various decoupling capacitors (e.g., 100nF, 10uF) and resistors (e.g., 10k, 1k, 100k) for voltage division and current limiting.
- Microcontroller:** The Pico-2 microcontroller is connected to various pins, including GPIOs, I2C, and SPI interfaces.
- Memory:** A 16MB SPI flash memory is connected to the microcontroller's SPI pins.
- Communication:** The schematic shows connections for I2C (SDA, SCL), SPI (MOSI, MISO, CS), and UART (TX, RX) interfaces.
- Other Components:** A 12V regulator (LDO12V) is present for higher voltage needs, and a 100k pull-up resistor is used for the I2C SDA line.

The schematic is overlaid with a large red watermark reading "https://t.me/schematics4laptop".

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ASSEMBLY  
PAGE DETAIL

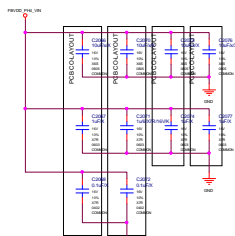
ASSEMBLY DESCRIPTION  
PS: FW/CO FW/2

**GIGABYTE**

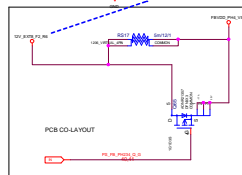
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Document Number  
GV-N3090AORUS X-24GD

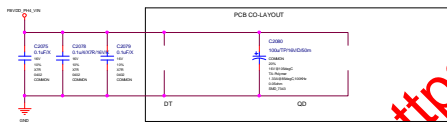
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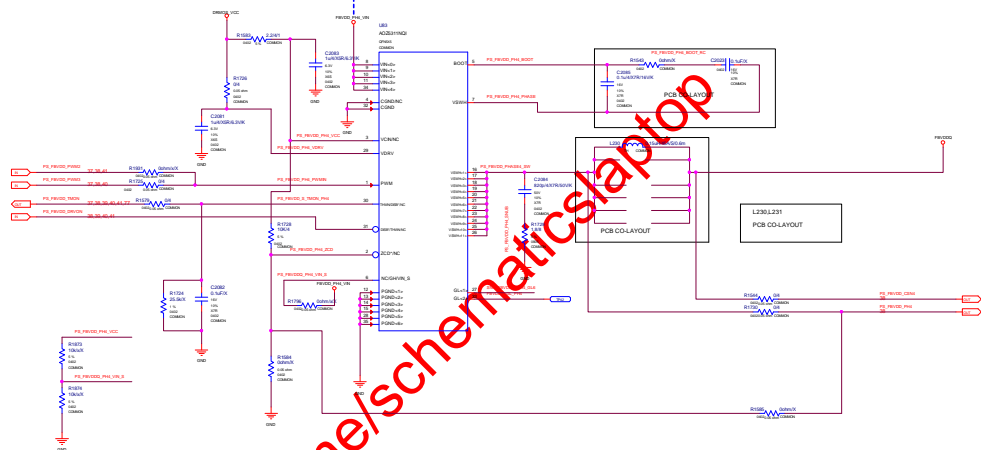
Add 8 Pin3, Change 12V rail.



## FBVDD PH3 INPUT ANTI-BACKDRIVE



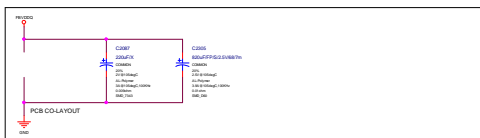
Add 8 Pin3, Change 12V rail.



<https://t.me/schematics4laptop>

## REFER TO PCB FOR BOM STUFFING

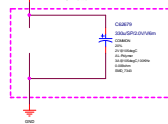
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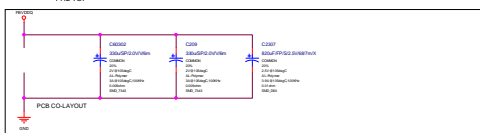
PH3 TOP



PH3 Bottom



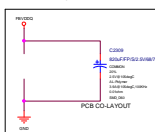
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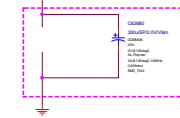
PH4 TOP



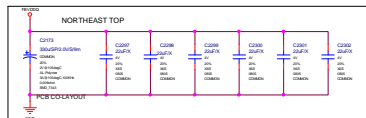
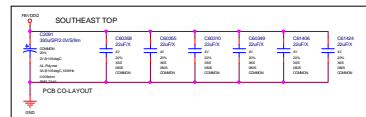
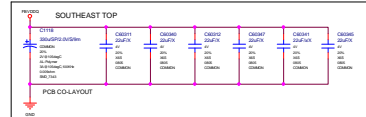
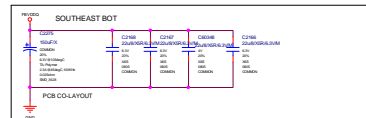
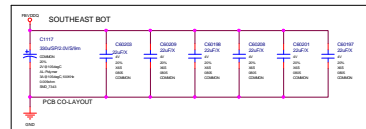
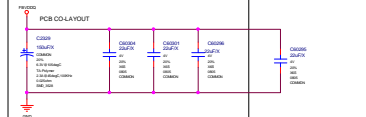
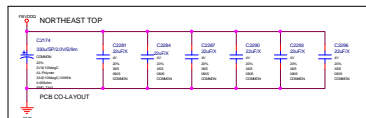
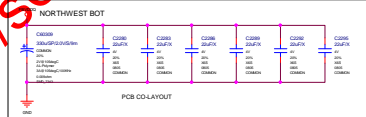
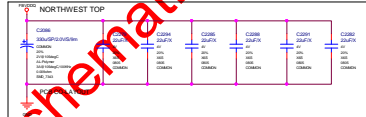
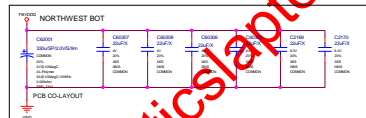
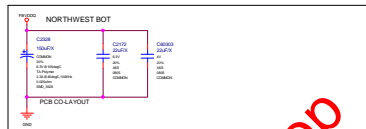
PH4 TOP



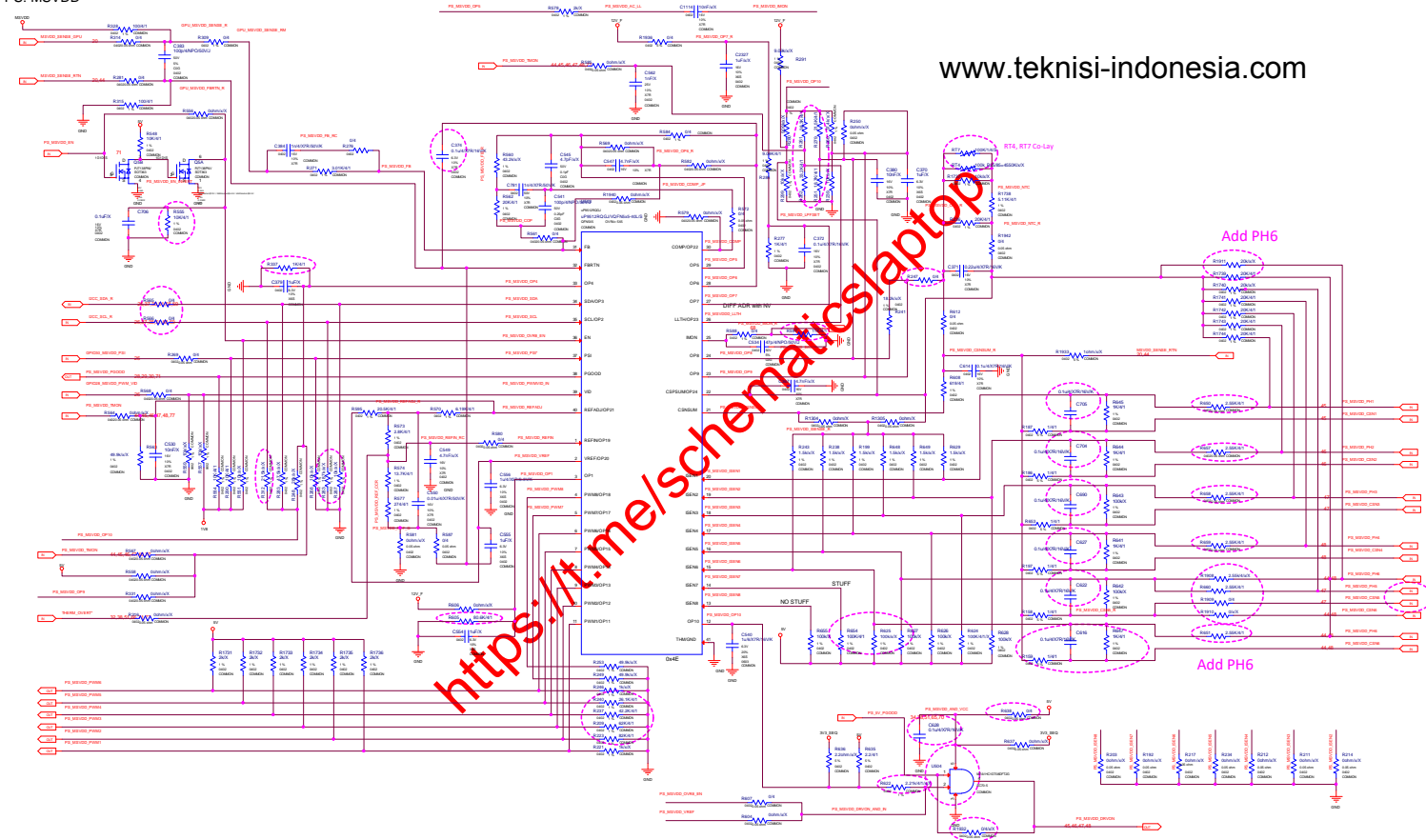
PH4 Bottom

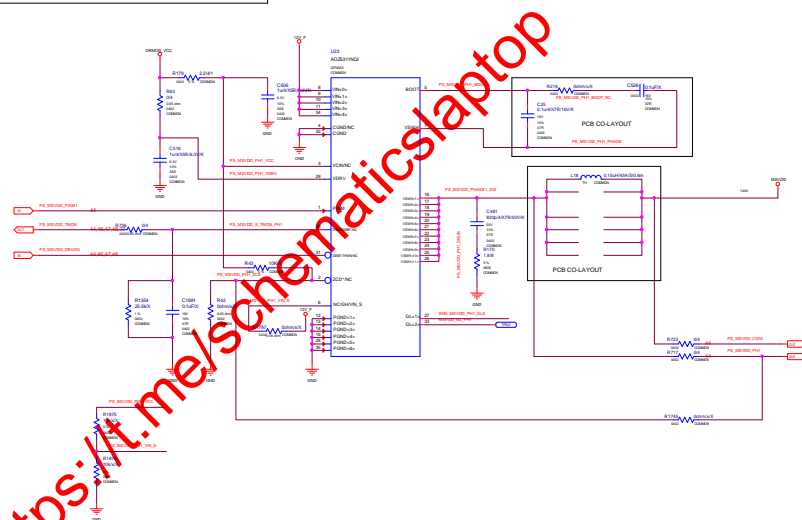
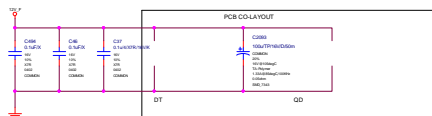
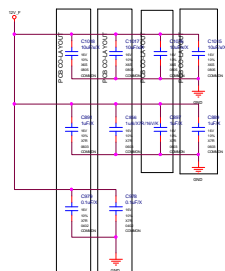


CLOSE TO PH3 PH4 OUTPUT STUFF

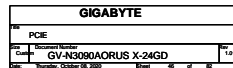


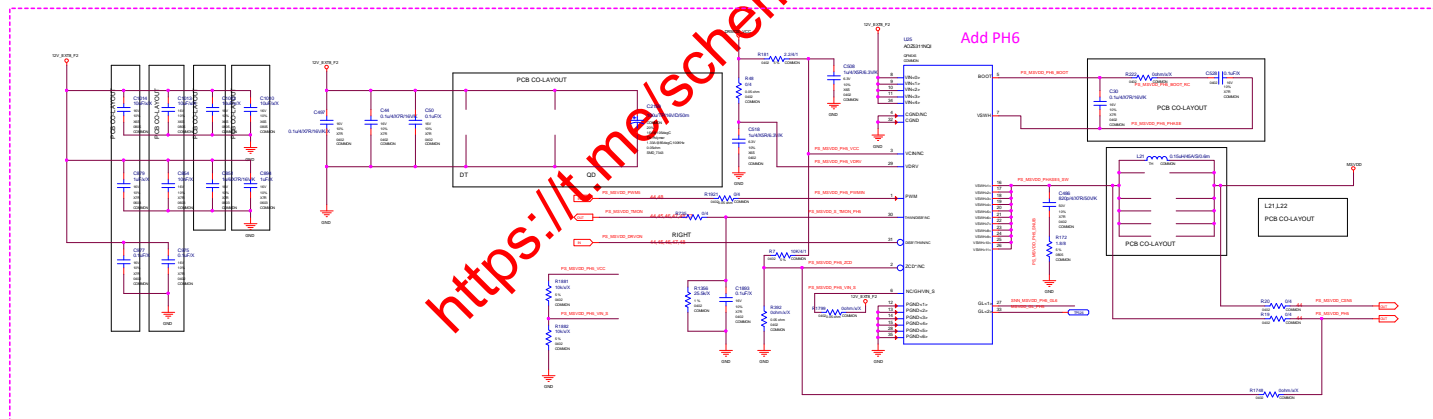
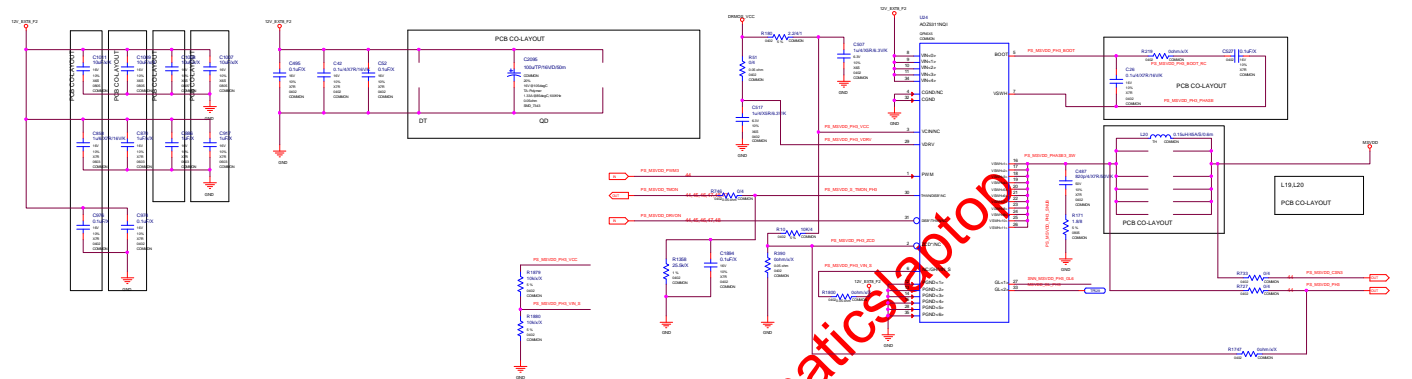
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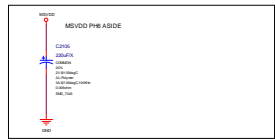
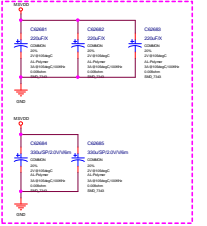
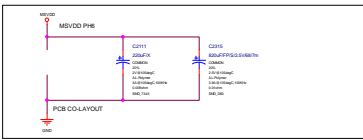
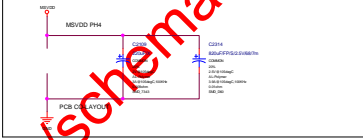
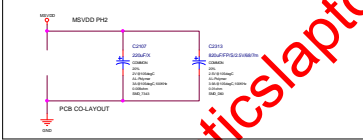
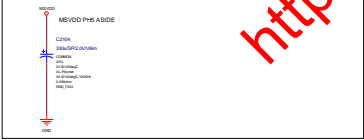
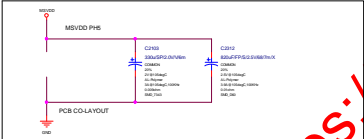
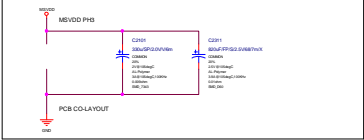
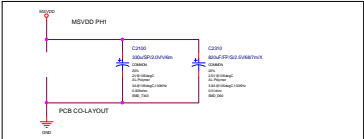








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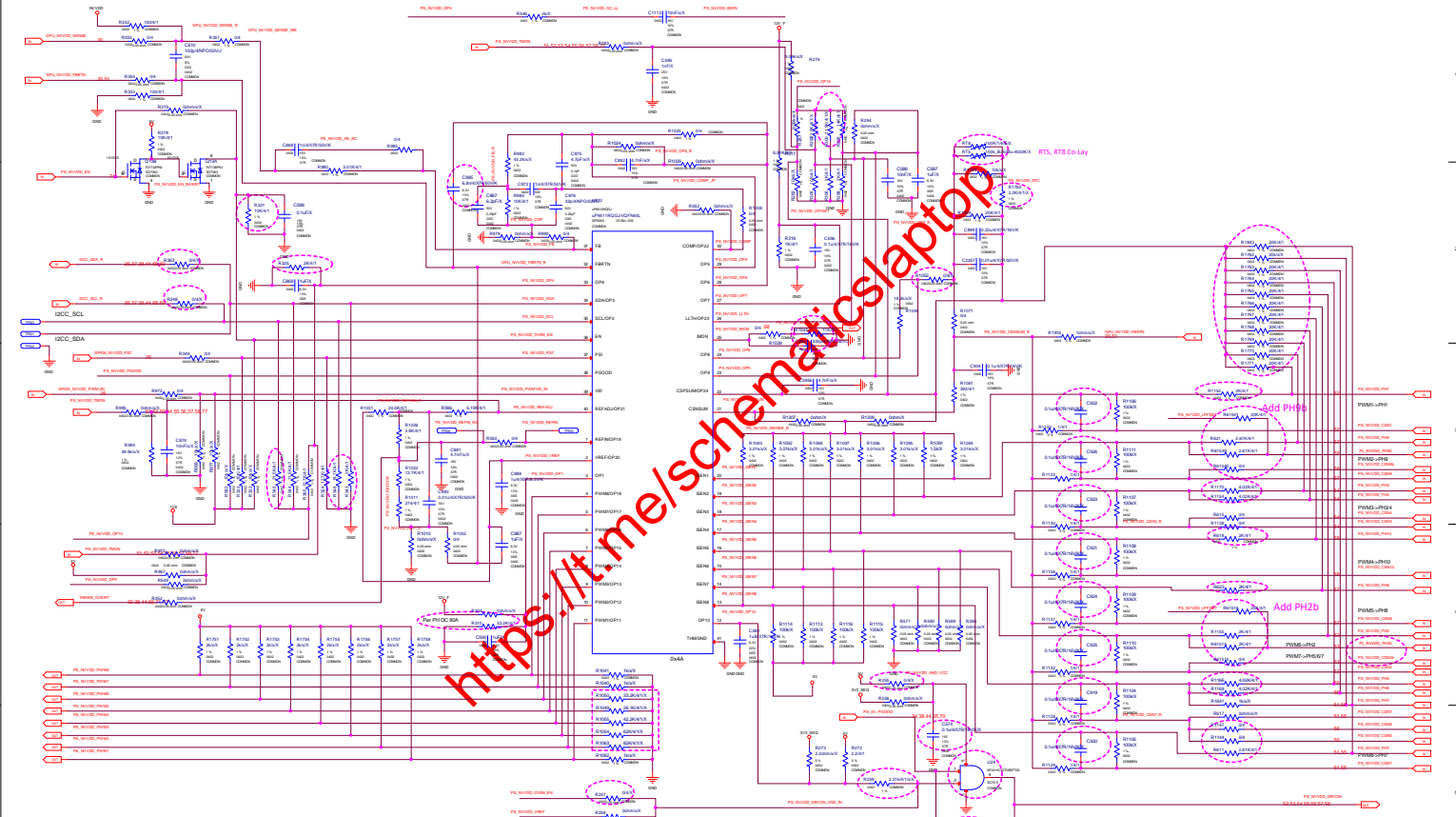
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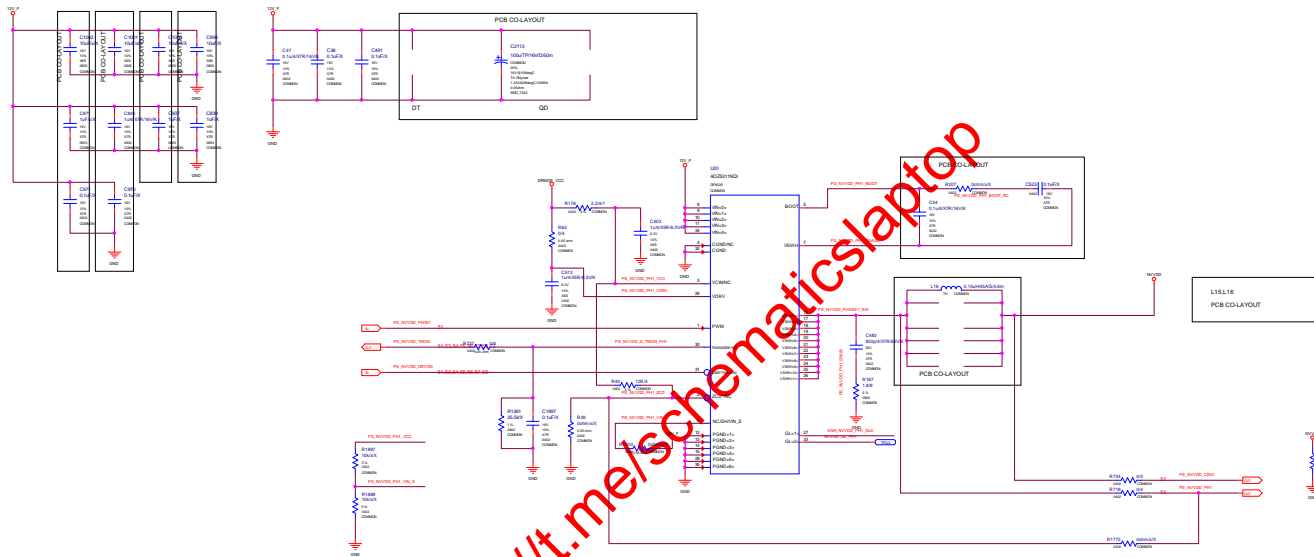
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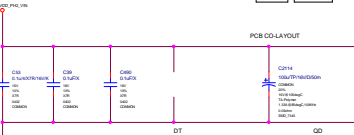
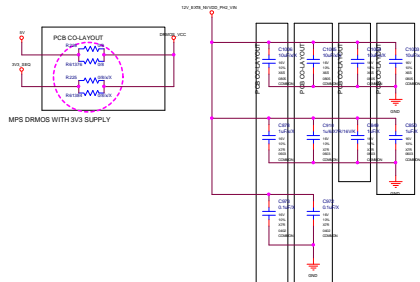
GIGABYTE	
PCIE	
GV-N3090AORUS X-24GD	
Rev: 1.00	Rev: 1.00

# PS: NVDD Control\_OVR8

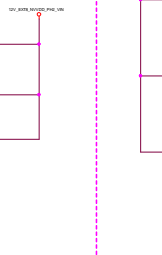




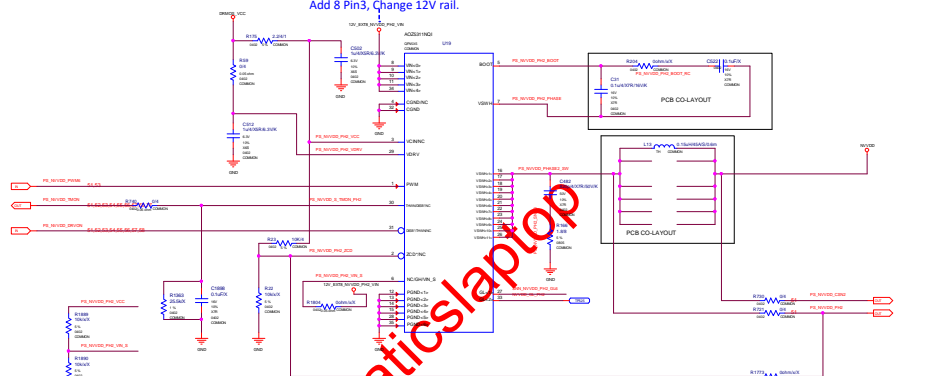
## PS: NVVDD Phase 2 (PWM6)



Add 8 Pin3, Change 12V rail.

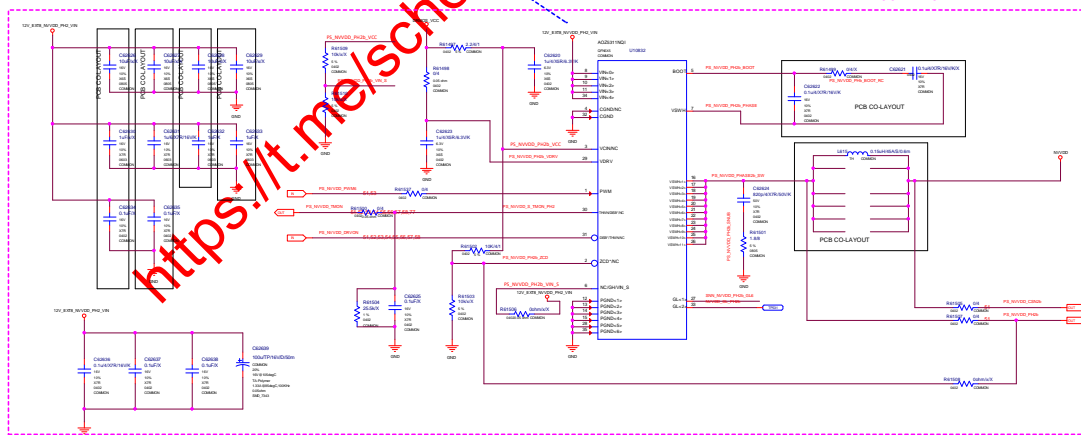


Add 8 Pin3, Change 12V rail.



Add 8 Pin3, Change 12V rail

Add PH2b



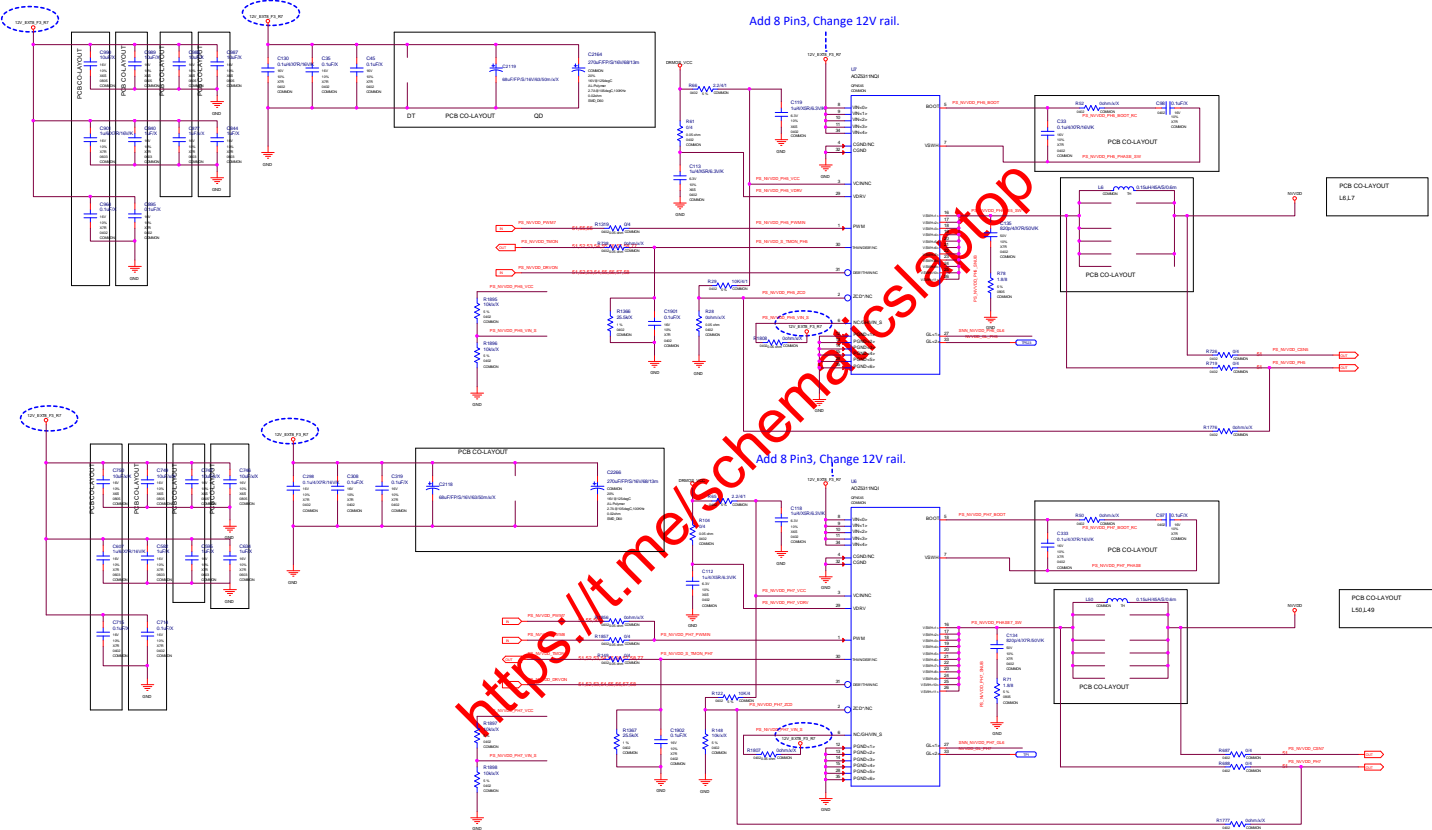
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Add 8 Pin3. Change 12V rail

## PS: NVVDD PH 5(PWM4), PH7(PWM8/4)



The schematic diagram illustrates the power management section of a Raspberry Pi 4B. It shows the CPU, RAM, and various peripheral chips like the USB controller, Ethernet controller, and audio codec. The diagram includes the power rails (VCC, GND) and the connections to the power pins on the board. A large red watermark 'https://t.me/schematics4rpi' is overlaid diagonally across the image.

Add 8 Pin3, Change 12V rail

Add 8 Pin3, Change 12V rail

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ASSEMBLY  
PAGE DETAIL

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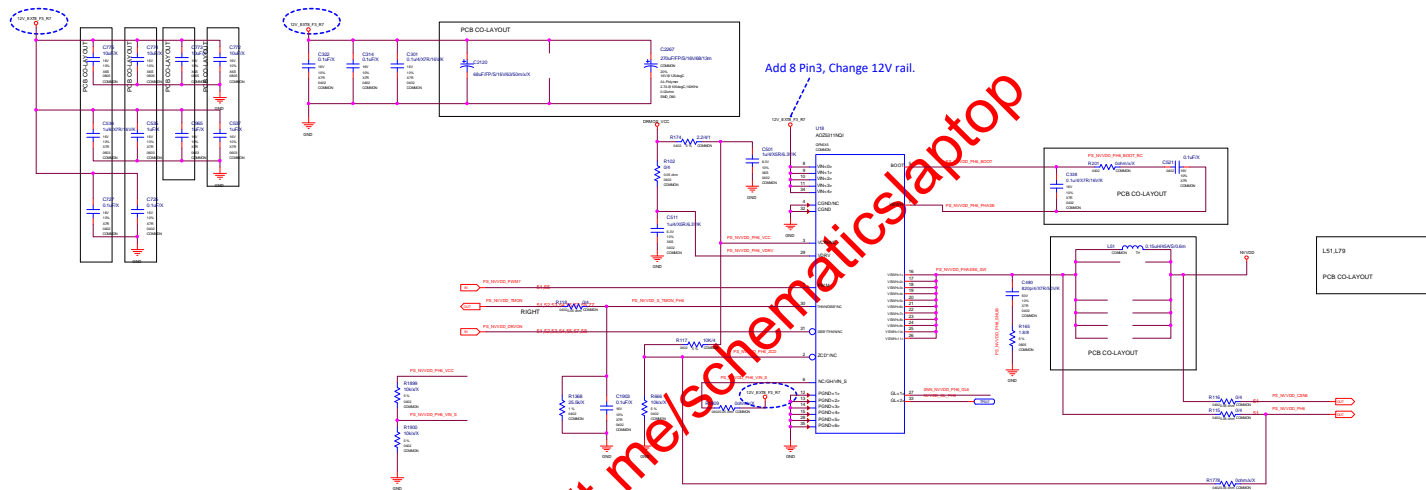
**GIGABYTE**

PCI

Document Number  
GV-N3090AORUS X-24GD

Level	1.0
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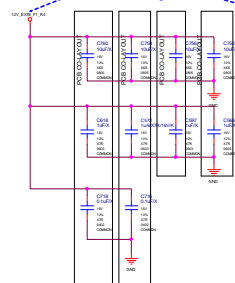
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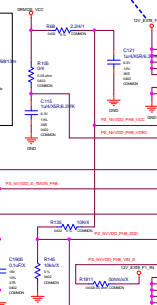


PS: NVVDD PH 8 (PWM5), PH 9(PWM2)

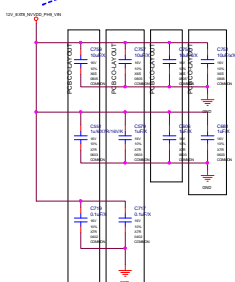
Add 8 Pin3, Change 12V rail.



Add 8 Pin3, Change 12V rail.

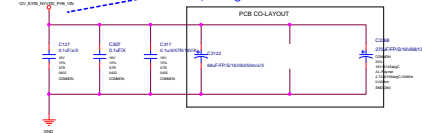


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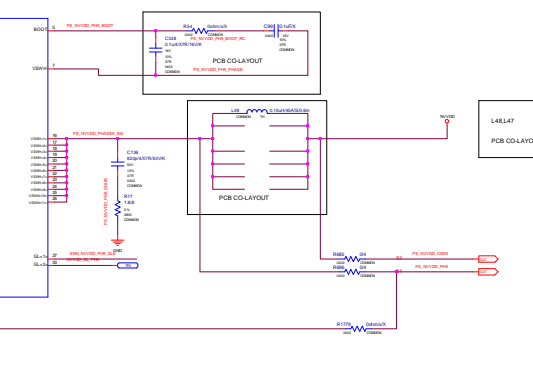
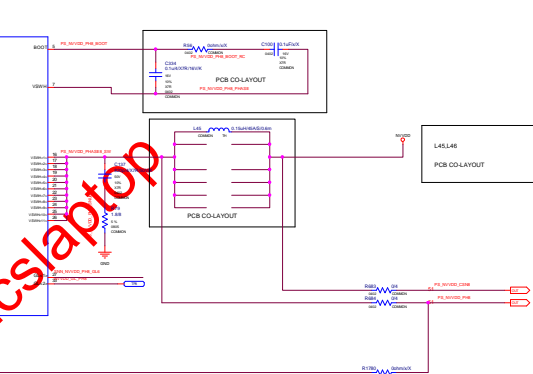


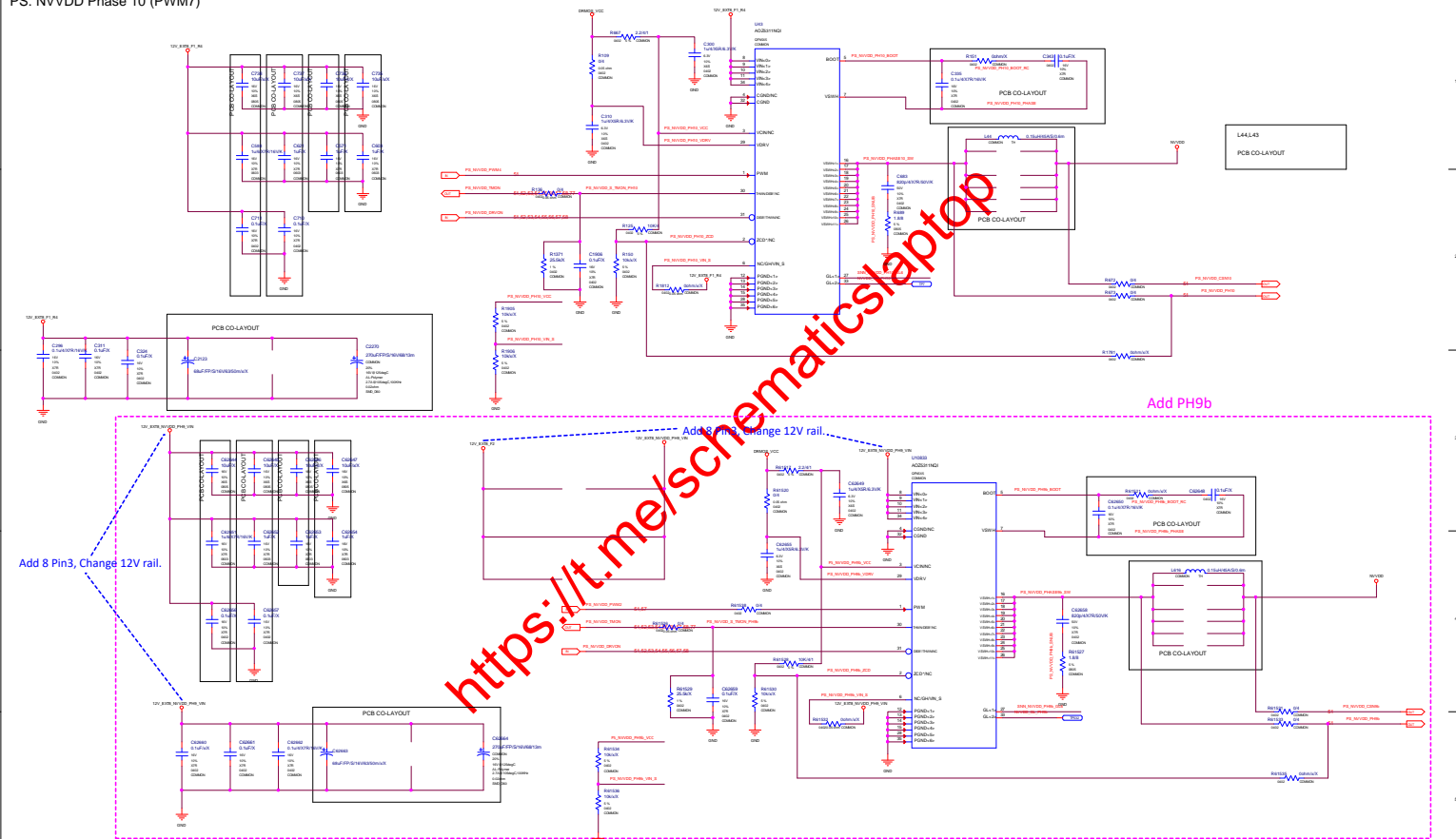
Add 8 Pin3, Change 12V rail.

Add 8 Pin3, Change 12V rail.



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ASSEMBLY

PAGE DETAIL

ASSEMBLY DESCRIPTION

Component Name

GIGABYTE	
PCIE	
GV-N3090AORUS X-24GD	
Rev 1.01	

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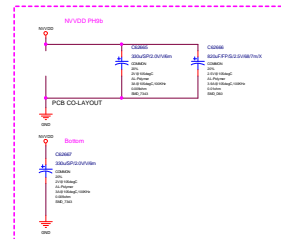
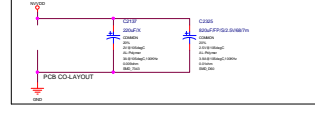
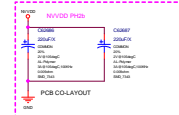
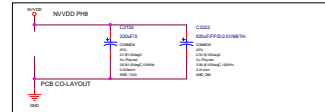
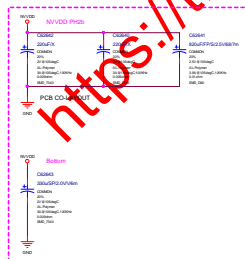
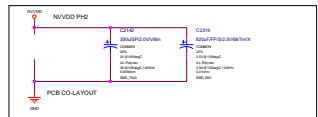
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ASSEMBLY PAGE DETAIL

ASSEMBLY DESCRIPTION

GIGABYTE	
PCIE	
GV-N3090AORUS X-24GD	
Rev 1.01	

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ASSEMBLY  
PAGE DETAIL

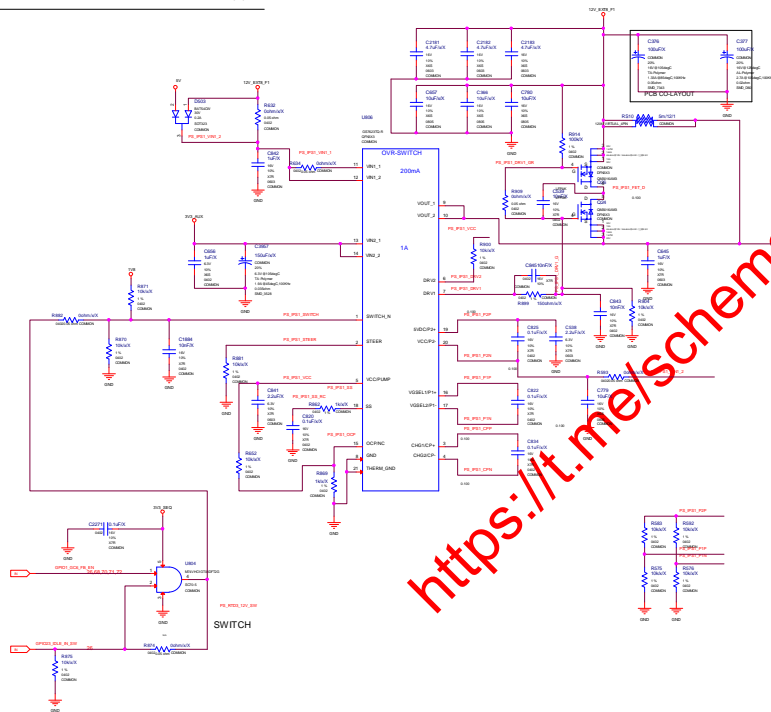
ASSEMBLY DESCRIPTION  
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GIGABYTE	
PCIE	
GV-N3090AORUS X-24GD	
Rev 1.01	

PS: INPUT SWITCH RTD3

#### AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
PS: INPUT SWITCH RT08

**GIGABYTE**

PCIE

Document Number  
GV-N2090AORUS Y-34GD

GV-N3090AORUS X-24GL		
Thursday, October 24, 2025		

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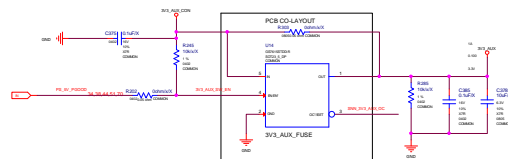
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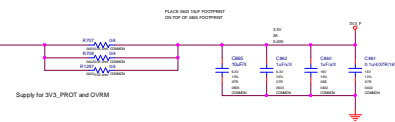
GIGABYTE	
PCIE	
GV-N3090AORUS X-24GD	
Rev 1.01	



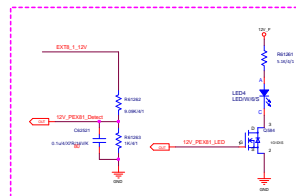
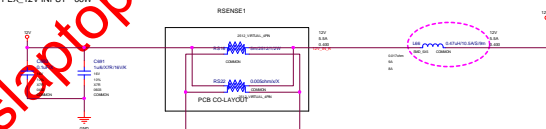
# PS: Inputs, Filtering, and Monitoring



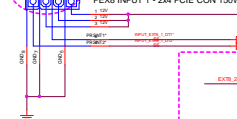
PEX 3V3 INPUT - 10W



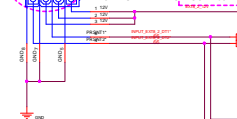
PEX 12V INPUT - 66W



PEXB INPUT 1 - 2x4 PCIe CON 150W

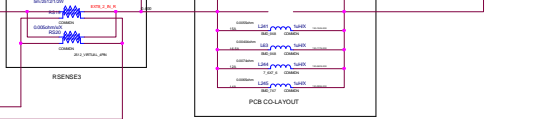
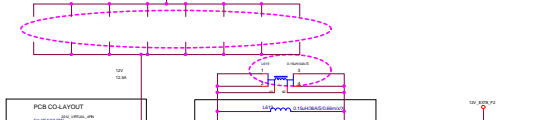
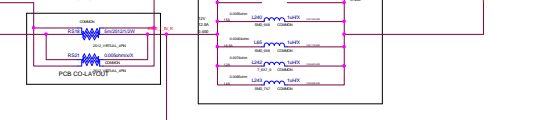


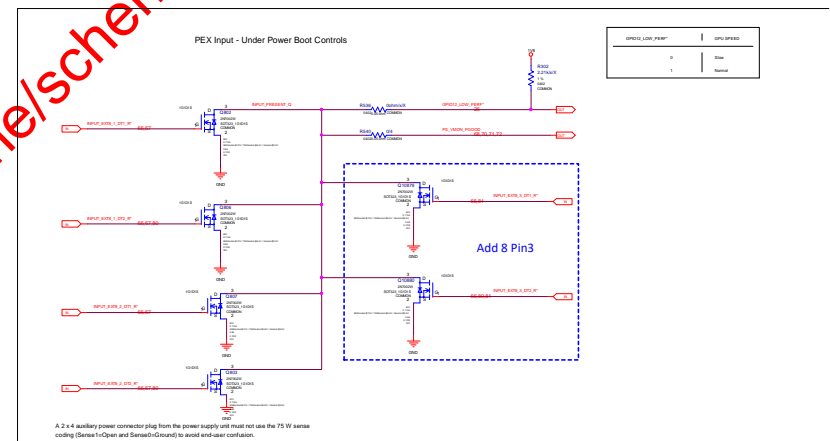
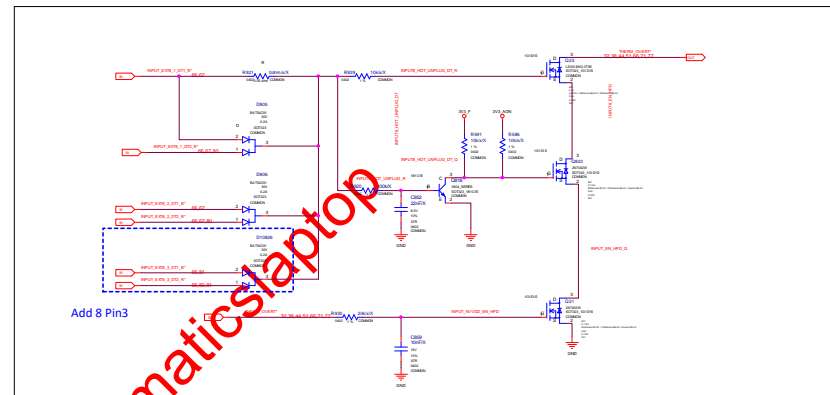
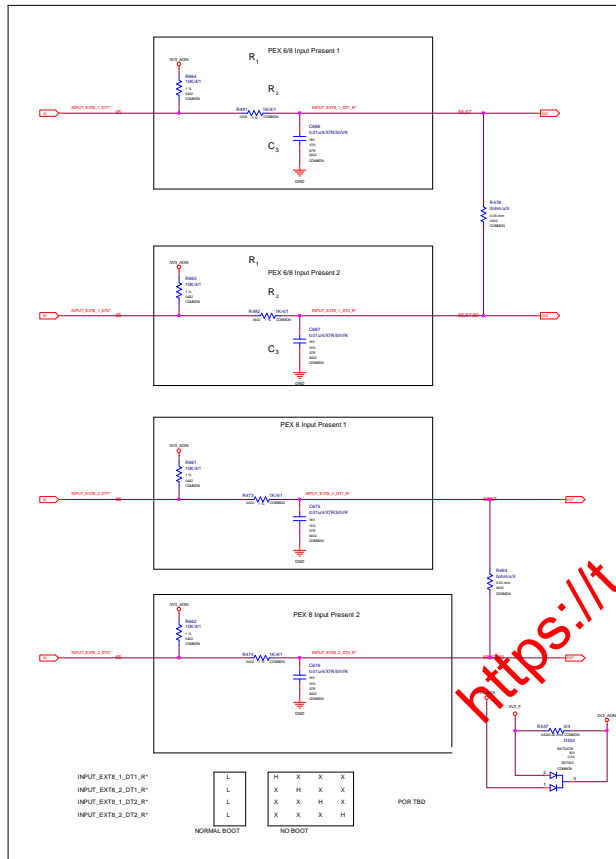
PEXB INPUT 2 - 2x4 PCIe CON 150W



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PEX 12V INPUT - 66W

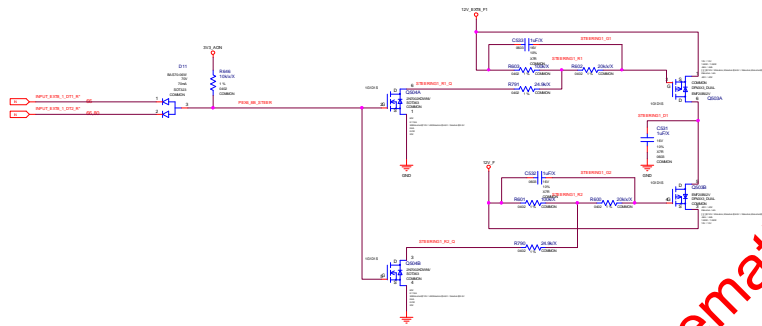




# PS: Discrete Steering

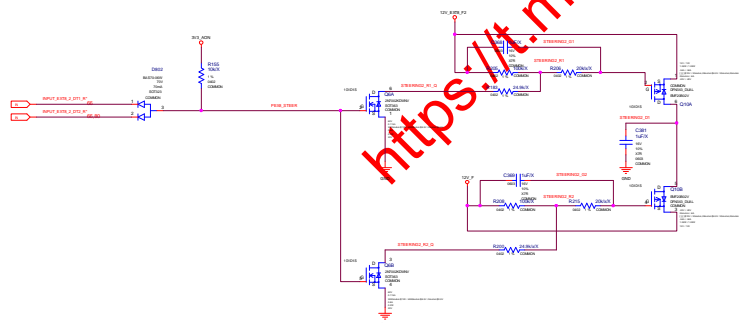
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V\_EXT8\_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V\_EXT8\_F2



www.teknisi-indonesia.com

# PS: Pre-Filter

Route the trace to PEX Golden Finger

05.00  
05.00

Add 8 Pin3

05.00  
05.00

05.00  
05.00

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05.00

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05.00  
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05.00  
05.00

STUFF IF USING DMMX

2.7V, 5.5V  
20V, 20V  
0.5A

0.5A

0.5A

0.5A

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Add 8 Pin3

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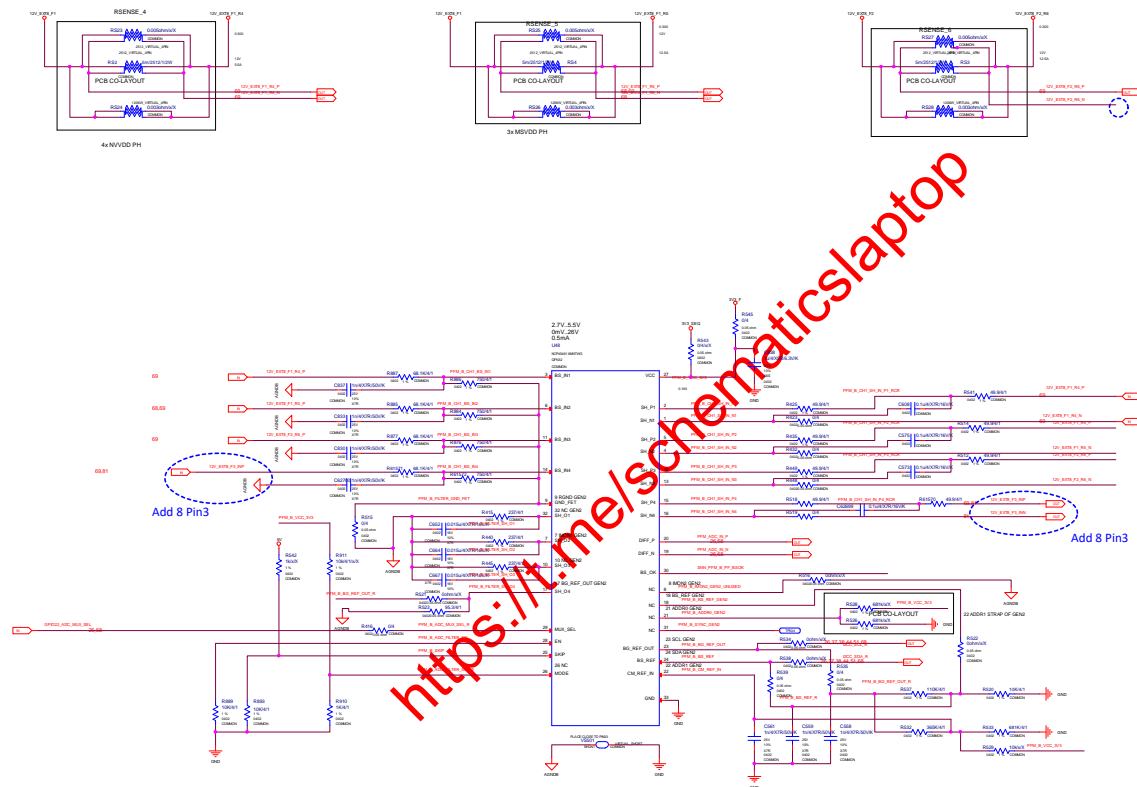
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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
PAGE PREVIEW

<b>GIGABYTE</b>	
PCIE	
GV-N3080AORUS X-24GD	
Model: N3080AORUS	

# PS: Pre-Filter B

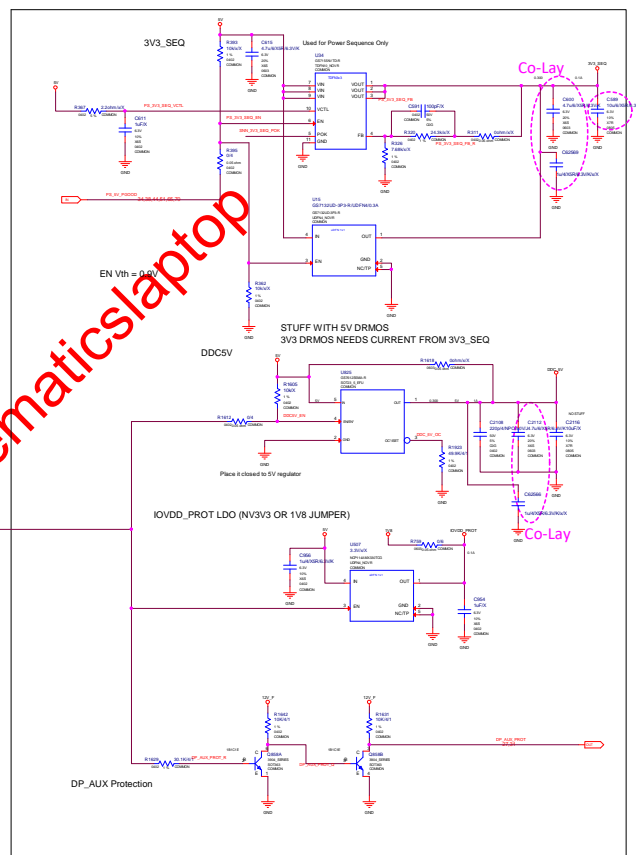
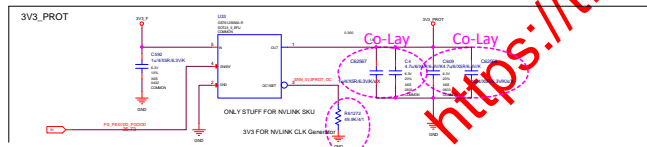
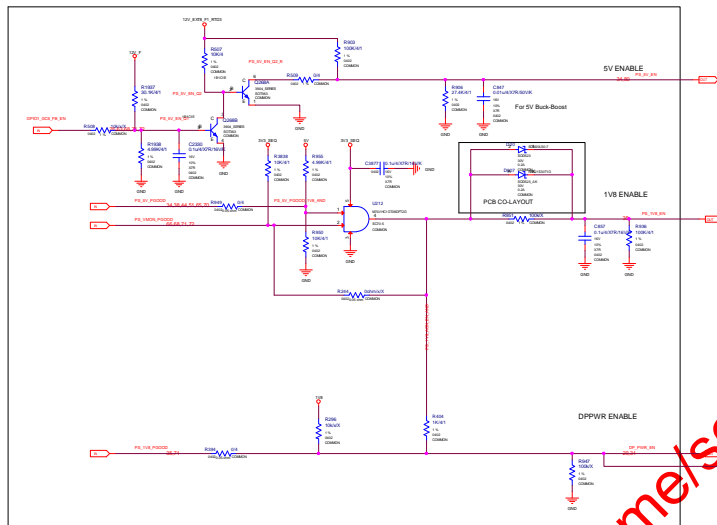


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ASSEMBLY PAGE DETAIL  
PS: PRE-FILTER B

<b>GIGABYTE</b>	
PCB	GV-N3080AORUS X-24GD
Model: GV-N3080AORUS X-24GD	Rev: 1.00

# SEQUENCE:5V,1V8,3V3\_SEQ ENABLE

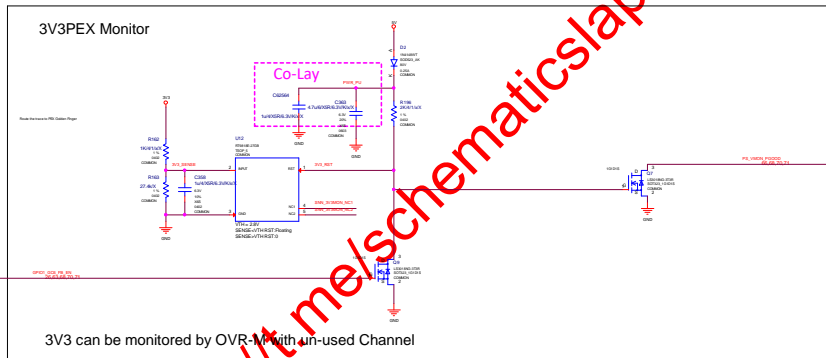


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ASSEMBLY DESCRIPTION  
Sequence No. PEX, F8 EN

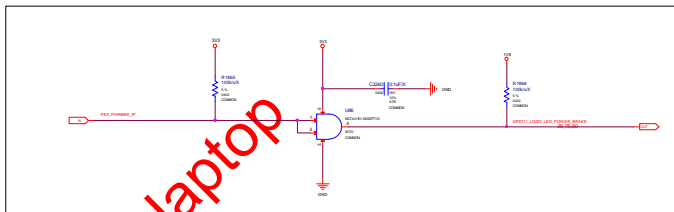
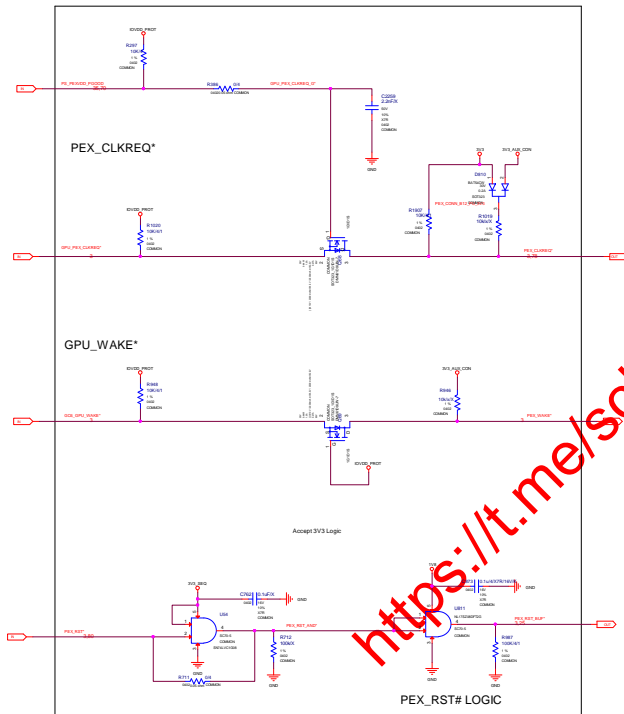
# Sequence: 3V3 MONITOR



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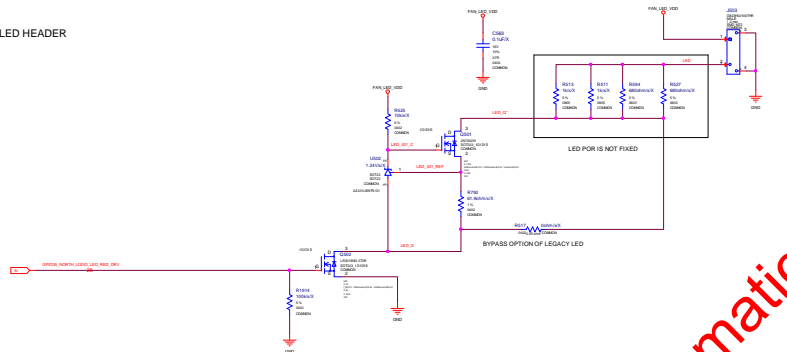
# SEQUENCE:MISC



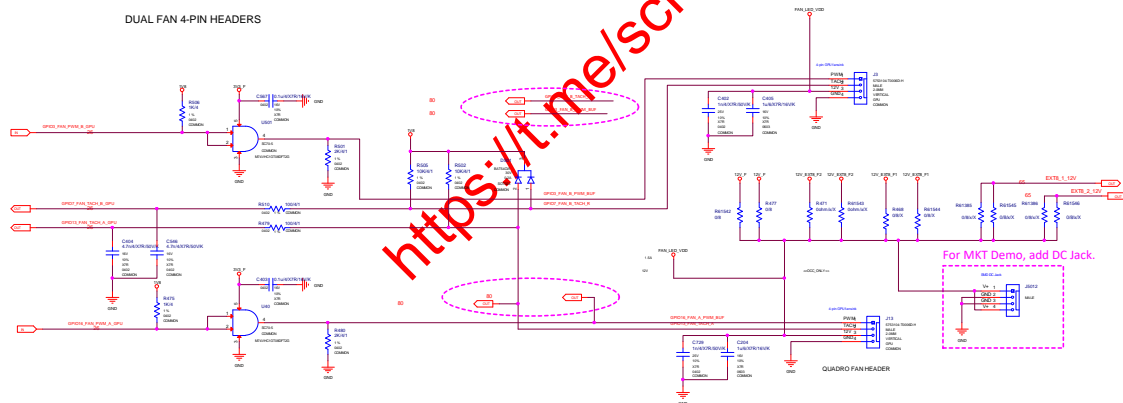
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MISC: LED & FAN

2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



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ASSEMBLY  
PAGE DETAIL

ASSEMBLY\_DESCRIPTION  
MSO\_LED & FAN

## GIGABYTE

PCIE

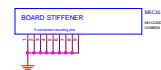
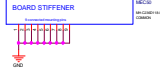
Document Number	GV-N3090AORUS X-24GD
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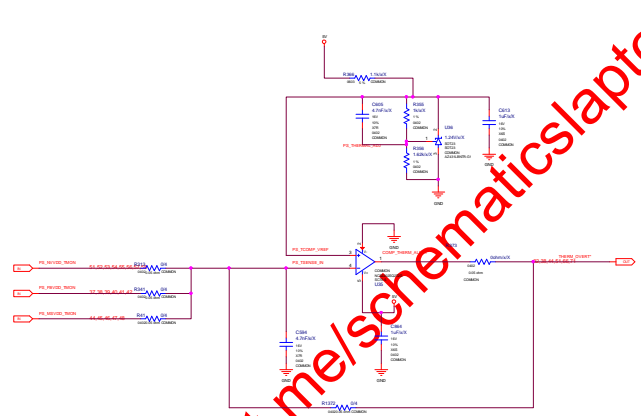


CONNECTOR SIZE TO FIT LAYOUT  
ALL CIRCUIT NO STUFF BY DEFAULT  
ALINGN WITH PASH  
IF ADDITIONAL POWER CONSUMPTION R  
NEEDED, IT SHOULD BE ON LED MOD.



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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
VR Thermal Protection

<b>GIGABYTE</b>	
PCE	
GV-N3080AORUS X-24GD	
Model: GV-N3080AORUS X-24GD	Rev: 1.00

PCI TERM



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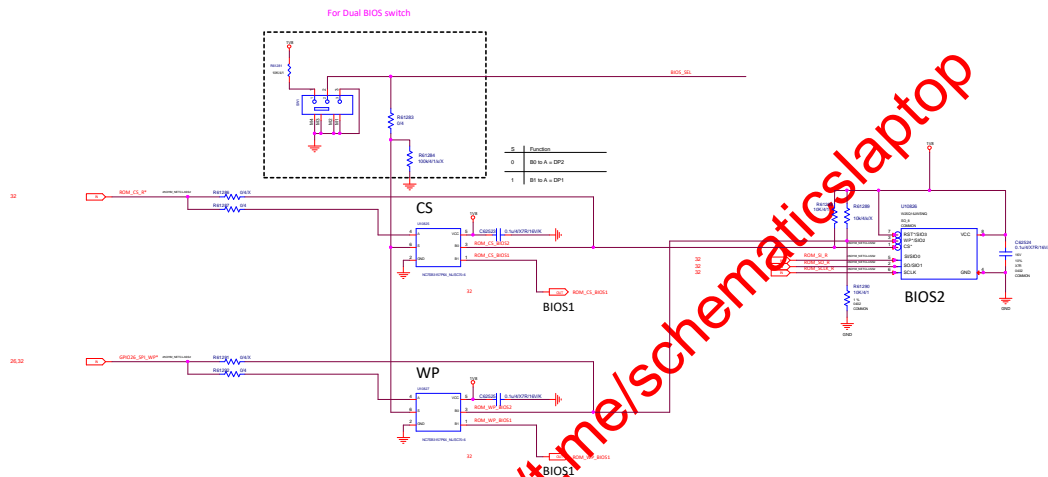
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ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
PCI TERM

GIGABYTE	
PCIE	
GV-N3080AORUS X-24GD	
Model: GV-N3080A-24GD	Rev: 1.00

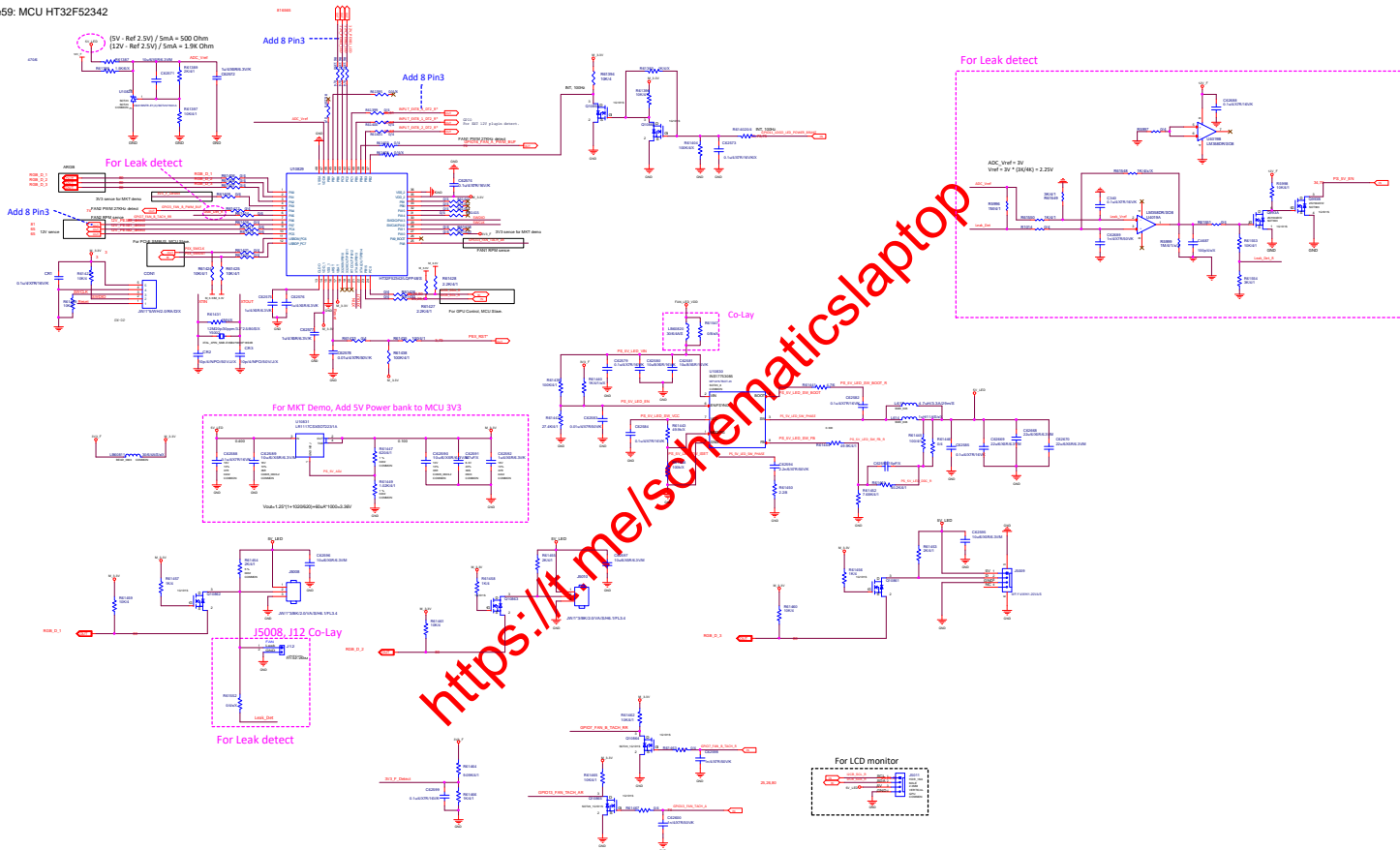
## BIOS Switch

[illegible]

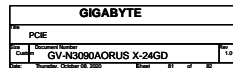
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ASSEMBLY  
PAGE DETAIL

ASSEMBLY\_DESCRIPTION  
MCUZERO POWER BLE







History

Date	Modify
2018.07.21	First version

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